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**UNITED STATES DISTRICT COURT  
 SOUTHERN DISTRICT OF NEW YORK**

In re: Adelphia Communications Corporation, et al.	)	Chapter 11
	)	
	)	Case No. 02-41729 (REG)
Debtors	)	Jointly Administered
	)	
Rembrandt Technologies, LP	)	
	)	Adversary Proceeding
<i>Plaintiff/Counter-defendants</i>	)	
	)	No. 06-01739 (REG)
v.	)	
	)	
Adelphia Communications Corporation;	)	
Century-TCI California, LP;	)	
Century-TCI California Communications, LP;	)	____ Civ. ____ ( )
Century-TCI Distribution Company, LLC;	)	
Century-TCI Holdings, LLC;	)	
Parnassos, LP;	)	
Parnassos Communications, LP;	)	
Parnassos Distribution Company I, LLC;	)	
Parnassos Distribution Company II, LLC;	)	
Parnassos Holdings, LLC;	)	
Western NY Cablevision, LP	)	
	)	
<i>Defendants/Counterclaimants</i>	)	

**DECLARATION OF MARC B. HANKIN IN SUPPORT  
 OF REMBRANDT TECHNOLOGIES, LP'S MOTION TO  
 WITHDRAW THE REFERENCE TO THE BANKRUPTCY COURT**

I, Marc B. Hankin, pursuant to 28 U.S.C. § 1746, hereby declare, under penalty of perjury:

1. I am an attorney with the firm of Shearman & Sterling LLP, co-counsel to Rembrandt Technologies, LP (“Rembrandt”), in connection with the above-captioned adversary proceeding (the “Adversary Proceeding”). I submit this Declaration in support of Rembrandt’s Motion to Withdraw the Reference to the Bankruptcy Court.

2. Attached hereto as Exhibit A is a true and correct copy of the Complaint for Post-Petition Patent Infringement filed by Rembrandt Technologies, LP against Adelphia Communications Corporation and certain of its subsidiaries and affiliates (collectively, the “Defendants”) in the Bankruptcy Court for the Southern District of New York (the “Bankruptcy Court”) on September 13, 2006.

3. Attached hereto as Exhibit B is a true and correct copy of the administrative expense claim filed by Rembrandt against the Defendants in the Bankruptcy Court on September 13, 2006.

4. Attached hereto as Exhibit C is a true and correct copy of the Defendants’ Answer, Affirmative Defenses and Counterclaims, dated November 27, 2006.

5. Attached hereto as Exhibit D is a true and correct copy of Rembrandt’s Reply to Defendants’ Answer and Counterclaims, dated December 15, 2006.

6. Attached hereto as Exhibit E is a true and correct copy of the Stipulated Order Establishing Separate Reserve for Rembrandt Technologies, LP Administrative Claim, dated December 13, 2006.

Dated: January 10, 2007

/s/ Marc B. Hankin  
Marc B. Hankin

**Exhibit A**



2. Defendant Adelphia Communications Corporation ("ACC") is a corporation organized under the laws of the State of Delaware. On June 25, 2002, ACC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York in a case captioned *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG). That case remains pending in the bankruptcy court. ACC's principal place of business on the Petition Date was located in Coudersport, Pennsylvania, and is currently located in Greenwood Village, Colorado. ACC was one of the leading cable and telecommunications companies in the United States. Since seeking bankruptcy protection on June 25, 2002, ACC continued to provide cable internet and television services to consumers throughout the United States until the sale of substantially all of its assets on July 31, 2006.

3. Defendant Century-TCI California, LP is a partnership organized under the laws of the State of Delaware. Century-TCI California, LP is an affiliate of ACC. On June 25, 2002, Century-TCI California, LP filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Century-TCI California, LP's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

4. Defendant Century-TCI California Communications, LP is a partnership organized under the laws of the State of Delaware. Century-TCI California Communications, LP is an affiliate of ACC. On June 25, 2002, Century-TCI California Communications, LP filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Century-TCI California Communications, LP's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

5. Defendant Century-TCI Distribution Company, LLC is a limited liability company organized under the laws of the State of Delaware. Century-TCI Distribution Company, LLC is an affiliate of ACC. On October 6, 2005, Century-TCI Distribution Company, LLC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Century-TCI Distribution Company, LLC's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

6. Defendant Century-TCI Holdings, LLC is a corporation organized under the laws of the State of Delaware. Century-TCI Holdings, LLC is an affiliate of ACC. On June 25, 2002, Century-TCI Holdings, LLC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Century-TCI Holdings, LLC's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

7. Defendant Parnassos Communications, LP is a partnership organized under the laws of the State of Delaware. Parnassos Communications, LP is an affiliate of ACC. On June 25, 2002, Parnassos Communications, LP filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Parnassos Communications, LP's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

8. Defendant Parnassos Distribution Company I, LLC is a limited liability company organized under the laws of the State of Delaware. Parnassos Distribution Company I, LLC is an affiliate of ACC. On October 6, 2005, Parnassos Distribution Company I, LLC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of

New York. Parnassos Distribution Company I, LLC's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

9. Defendant Parnassos Distribution Company II, LLC is a limited liability company organized under the laws of the State of Delaware. Parnassos Distribution Company II, LLC is an affiliate of ACC. On October 6, 2005, Parnassos Distribution Company II, LLC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Parnassos Distribution Company II, LLC's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

10. Defendant Parnassos Holdings, LLC is a corporation organized under the laws of the State of Delaware. Parnassos Holdings, LLC is an affiliate of ACC. On June 25, 2002, Parnassos Holdings, LLC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Parnassos Holdings, LLC's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

11. Defendant Parnassos, LP is a partnership organized under the laws of the State of Delaware. Parnassos, LP is an affiliate of ACC. On June 25, 2002, Parnassos, LP filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Parnassos, LP's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

12. Defendant Western NY Cablevision, LP is a partnership organized under the laws of the State of Delaware. Western NY Cablevision, LP is an affiliate of ACC. On June 25, 2002, Western NY Cablevision, LP filed a petition in bankruptcy under Chapter 11 in the United

States Bankruptcy Court for the Southern District of New York. Western NY Cablevision, LP's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

13. On information and belief, Defendants are liable for the infringement of Rembrandt's patents as alleged herein. Rembrandt makes these allegations with regard to particular Defendants based on a review of publicly available information. Other affiliates of ACC may also be liable for infringement of these patents. Rembrandt intends to amend this pleading to add other ACC affiliates who have infringed Rembrandt's patents or, if appropriate, to dismiss Defendants who are shown not to have engaged in any infringing activity.

#### **JURISDICTION AND VENUE**

14. This is an action for patent infringement arising under the law of the United States relating to patents, including, *inter alia*, 35 U.S.C. §§ 271, 281, 284 and 285. This court has jurisdiction over such federal question claims pursuant to 28 U.S.C. §§ 1331 and 1338(a).

15. For the avoidance of doubt and for the sake of clarity, Plaintiffs hereby explicitly state that all acts of infringement alleged herein relate solely to actions taken by Defendants *after* their filing for bankruptcy in this district on June 25, 2002 or October 6, 2005, as applicable, and *before* the acquisition by Time Warner Cable and Comcast on July 31, 2006 (such period for each Defendant, the "Post-Petition Period"). Plaintiffs hereby explicitly state and affirm that they are not seeking relief for any actions of Defendants that occurred prior to the filing of ACC's bankruptcy petition. ACC continued to operate its cable internet and television businesses after June 25, 2002 and prior to its acquisition. In doing so, as alleged in greater detail below, ACC engaged in post-petition acts of infringement that have damaged Rembrandt.

It is solely based on these post-petition actions, and for relief under the United States patent laws, that Rembrandt brings this action.

16. This Court has personal jurisdiction over the Defendants because one or more events giving rise to the causes of action herein occurred in this district and because the Defendants have submitted to the jurisdiction of this Court.

17. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b) and 1409(a).

**COUNT I: INFRINGEMENT OF U.S. PATENT NO. 5,710,761**

18. Rembrandt refers to and incorporates herein the allegations of Paragraphs 1-17 above.

19. Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 5,710,761, entitled "Error Control Negotiation Based on Modulation" ("the '761 patent."). A true copy of the '761 patent is attached as Exhibit A.

20. The '761 patent was duly and legally issued by the United States Patent and Trademark Office on January 20, 1998, after full and fair examination.

21. During the Post-Petition Period, the Defendants have directly or indirectly infringed the '761 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '761 patent, in this district and otherwise within the United States. For example, Defendants infringed the '761 patent by providing high-speed cable modem internet products and services to subscribers.

22. Rembrandt suffered substantial damages due to the Defendants' infringement. Furthermore, upon information and belief, such infringement was willful, making this an

exceptional case and entitling Rembrandt to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

**COUNT II: INFRINGEMENT OF U.S. PATENT NO. 5,778,234**

23. Rembrandt refers to and incorporates herein the allegations of Paragraphs 1-17 above.

24. Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 5,778,234, entitled "Method for Downloading Programs" ("the '234 patent."). A true copy of the '234 patent is attached as Exhibit B.

25. The '234 patent was duly and legally issued by the United States Patent and Trademark Office on July 7, 1998, after full and fair examination.

26. During the Post-Petition Period, the Defendants have directly or indirectly infringed the '234 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '234 patent, in this district and otherwise within the United States. For example, the Defendants infringed the '234 patent by providing high-speed cable modem internet products and services to subscribers.

27. Rembrandt suffered substantial damages due to the Defendants' infringement. Furthermore, upon information and belief, such infringement was willful, making this an exceptional case and entitling Rembrandt to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

**COUNT III: INFRINGEMENT OF U.S. PATENT NO. 6,131,159**

28. Rembrandt refers to and incorporates herein the allegations of Paragraphs 1-17 above.

29. Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 6,131,159, entitled "System for Downloading Programs" ("the '159 patent."). A true copy of the '159 patent is attached as Exhibit C.

30. The '159 patent was duly and legally issued by the United States Patent and Trademark Office on October 10, 2000, after full and fair examination.

31. During the Post-Petition Period, the Defendants have directly or indirectly infringed the '159 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '159 patent, in this district and otherwise within the United States. For example, the Defendants infringed the '159 patent by providing high-speed cable modem internet products and services to subscribers.

32. Rembrandt suffered substantial damages due to the Defendants' infringement. Furthermore, upon information and belief, such infringement was willful, making this an exceptional case and entitling Rembrandt to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

**COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 6,950,444**

33. Rembrandt refers to and incorporates herein the allegations of Paragraphs 1-17 above.

34. Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 6,950,444, entitled "System and Method for a Robust Preamble and Transmission Delimiting in a Switched-Carrier Transceiver" ("the '444 patent."). A true copy of the '444 patent is attached as Exhibit D.

35. The '444 patent was duly and legally issued by the United States Patent and Trademark Office on September 27, 2005, after full and fair examination.

36. During the Post-Petition Period, Defendants directly or indirectly infringed the '444 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '444 patent, in this district and otherwise within the United States. For example, the Defendants infringed the '444 patent by providing high-speed cable modem internet products and services to subscribers.

37. Rembrandt suffered substantial damages due to the Defendants' infringement. Furthermore, upon information and belief, such infringement was willful, making this an exceptional case and entitling Rembrandt to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

#### **PRAYER FOR RELIEF**

WHEREFORE, Rembrandt prays that it have judgment from the District Court against the Defendants for the following:

- (1) An order that the Defendants have infringed the patents-in-suit;
- (2) An award of damages for said infringement;
- (4) An award of increased damages pursuant to 35 U.S.C. § 284;
- (5) An award of all costs of this action, including attorneys' fees and interest; and
- (6) Such other and further relief, at law or in equity, to which Rembrandt is justly entitled.

Dated: September 13, 2006.

**SUSMAN GODFREY L.L.P.**

By: /s/ Vineet Bhatia

VINEET BHATIA (VB 9964)

MAX L. TRIBBLE, JR.

Texas Bar 20213950 (*application pending*)

EDGAR SARGENT

Washington Bar 28283 (*application pending*)

BROOKE A.M. TAYLOR

Washington Bar 33190 (*application pending*)

TIBOR L. NAGY

Texas Bar 24041562 (*application pending*)

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**Exhibit A**



US005710761A

**United States Patent** [19]  
**Scott**

[11] **Patent Number:** **5,710,761**  
[45] **Date of Patent:** **Jan. 20, 1998**

[54] **ERROR CONTROL NEGOTIATION BASED ON MODULATION**

5,550,881 8/1996 Sridhar et al. 375/222  
5,636,037 6/1997 Smith 375/222

[75] **Inventor:** Robert Earl Scott, Indian Rocks Beach, Fla.

*Primary Examiner—Melvin Marcelo*  
*Attorney, Agent, or Firm—Thomas, Kayden, Horstemeier & Risley*

[73] **Assignee:** Paradyne Corporation, Largo, Fla.

[57] **ABSTRACT**

[21] **Appl. No.:** 458,048

[22] **Filed:** May 31, 1995

[51] **Int. Cl.<sup>6</sup>** H04L 1/00

[52] **U.S. Cl.** 370/252; 375/222; 379/93.08

[58] **Field of Search** 370/252, 465, 370/466, 467, 469; 375/222; 379/93

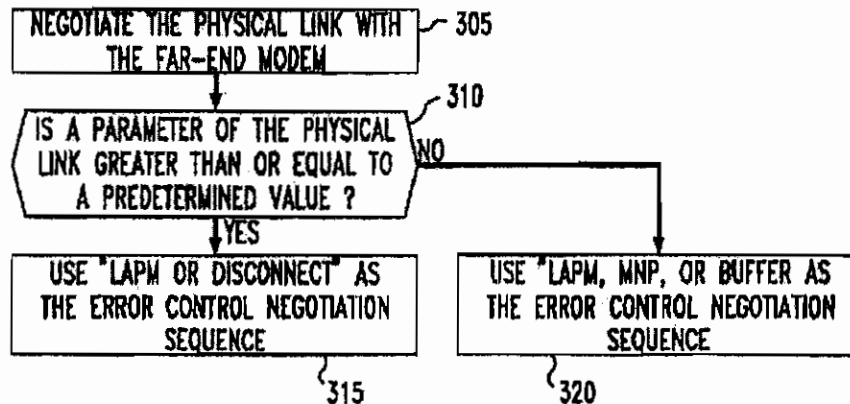
[56] **References Cited**

**U.S. PATENT DOCUMENTS**

4,715,044 12/1987 Gartner 375/8  
5,384,780 1/1995 Lomp et al. 375/222  
5,430,793 7/1995 Uetzel et al. 375/222  
5,481,696 1/1996 Lomp et al. 395/300

A modem dynamically selects the type of error-control negotiation sequence as a function of a negotiated parameter of the physical layer. In one embodiment of the invention, a modem selects between error-control negotiation sequences as a function of the type of modulation negotiated in the physical layer. In particular, the modem has at least two type of error-control negotiation sequences to select from: "LAPM or Disconnect," and "LAPM, MNP or Buffer." When the modem negotiates a V32 or higher modulation, the modem uses the "LAPM or Disconnect" error control negotiation sequence. However, when the modem negotiates a V22 bis or lower modulation, the modem uses the "LAPM, MNP or Buffer" error control sequence.

16 Claims, 1 Drawing Sheet



U.S. Patent

Jan. 20, 1998

5,710,761

FIG. 1

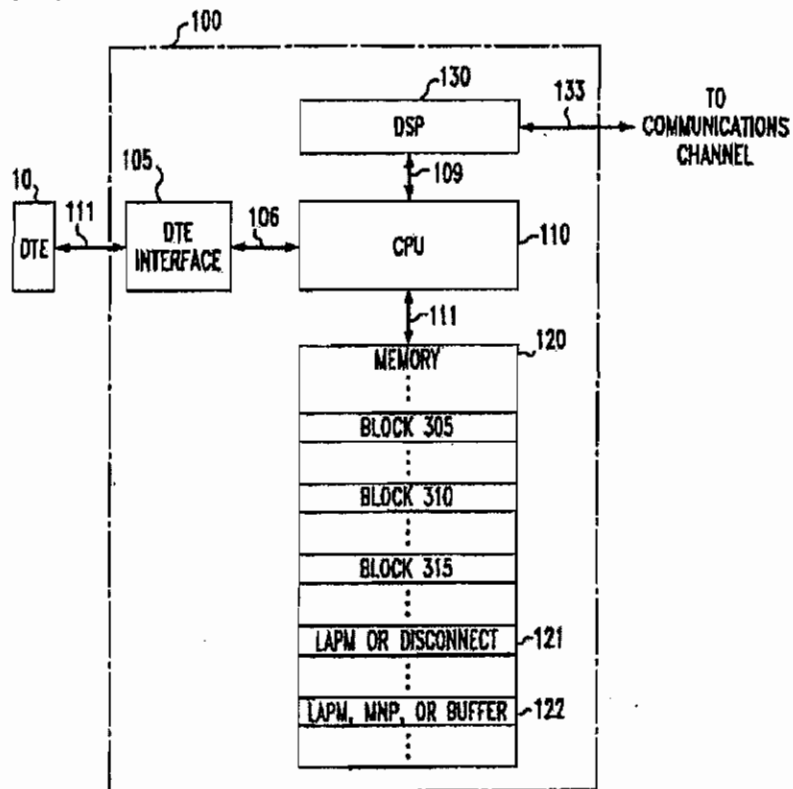
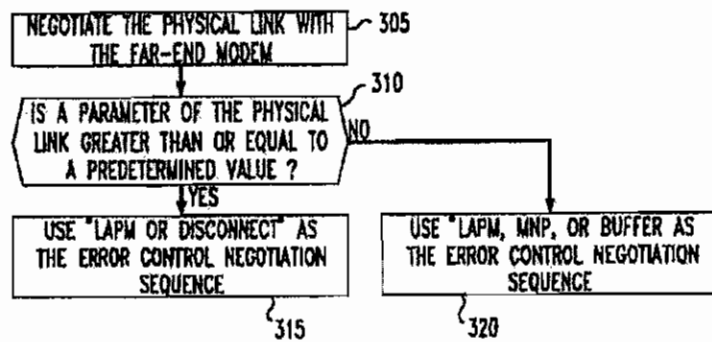


FIG. 2



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## ERROR CONTROL NEGOTIATION BASED ON MODULATION

### BACKGROUND OF THE INVENTION

The present invention relates to data communications equipment, e.g., modems, and, more particularly, to the error control negotiation phase of establishing a data connection.

In establishing a data connection between two modems, the modems perform a "handshaking" sequence to negotiate various parameters about the data connection, e.g., the type of modulation (which relates to line speed), and the type of error control protocol. The type of modulation is representative of the "physical" layer of a data connection, while the type of error control protocol is representative of the "link" layer of the data connection. The negotiation of the physical layer is always negotiated before the link layer.

The types of error control protocols used today are: "Link Access Protocol Modem" (LAPM), "Microcom Networking Protocol" (MNP), or "Buffer" (which in reality is no error control). Typically, in negotiating the type of error control protocol a modem tries each type of error control protocol in turn. In particular, the modem uses a negotiation sequence defined herein as "LAPM, MNP, or Buffer." In this negotiation sequence, the modem attempts to connect with the far-end modem for several seconds, e.g., 2 seconds, using an "LAPM" protocol like International Telecommunication Union (ITU) standard V.42. If the far-end modem does not appropriately respond, the modem then tries to connect with the far-end modem for several seconds, e.g., 6 seconds, using the "MNP" protocol. If this too is unsuccessful, the modem then falls back to a non-error control mode, i.e., the "Buffer" mode of operation. This type of negotiation sequence typically allows a modem to connect to the widest range of industry-available modems.

Unfortunately with higher modulation speeds available, like those in ITU standards V.34 and, to a lesser degree, V.32bis, the above error control negotiation sequence can present a problem. In particular, as noted above, the negotiation of the line speed (modulation) occurs before the negotiation of the type of error control. In order to determine the appropriate line speed, a modem uses a technique called "line probing." Unfortunately, the accuracy of current line probing techniques is not perfect. As a result, a modem may erroneously connect at too high a line speed. In other words, even though the line speed was successfully negotiated, the error rate at that line speed is high. This affects the time it takes to perform the subsequent error control negotiation. In particular, with an increase in the error rate, the LAPM type of error control may not be negotiated within the 2 seconds, mentioned above. Further, in severe cases, the time delay in negotiating the error control protocol will be so long that neither LAPM nor MNP is negotiated, causing the modem to fallback to buffer mode. The latter presents a problem, since users typically want V.42 error control and V.42bis data compression for their data calls, however in buffer mode neither V.42 error control nor V.42bis data compression are available.

One way to solve the above-mentioned problem is to have a different negotiation sequence for error control negotiation—"LAPM or Disconnect" for example. With this negotiation setting, the modem tries for an extended length of time, e.g., 30 seconds, to negotiate a LAPM data connection. Even if the modem has trouble at the start of the call, LAPM may still be negotiated because of the longer time delay. However, this negotiation sequence presents a problem when connecting to modems that do not support

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LAPM, i.e., MNP-only or non-error-control modems. In order to connect to MNP-only or non-error-control modems, the user must switch the modem back to using the "LAPM, MNP, or Buffer" error control negotiation sequence, described above. Typically, the user switches between error control negotiation sequences via an AT command. This is not user-friendly. In today's marketplace, the configuration of the modem itself, e.g., what type of error control negotiation sequence to use, should be transparent to the user.

### SUMMARY OF THE INVENTION

However, I have realized a solution that solves all of the above problems and is user-friendly. I have observed that almost every high-speed modem (V.34, V.32bis, V.32) has a LAPM mode, and that the LAPM mode is enabled. Further, only the low-speed modems (V.22bis or below) are MNP-only or non-error control. And, finally, the modulation (physical layer) is always negotiated before the error control protocol (link layer). Therefore, and in accordance with the invention, a modem dynamically selects the type of link layer negotiation sequence as a function of a negotiated parameter of the physical layer.

In one embodiment of the invention, a modem selects between error control negotiation sequences as a function of the type of modulation negotiated in the physical layer. In particular, the modem has at least two type of error control negotiation sequences to select from: "LAPM or Disconnect," and "LAPM, MNP or Buffer." When the modem negotiates a V.32 or higher modulation, the modem uses the "LAPM or Disconnect" error control negotiation sequence. However, when the modem negotiates a V.22bis or lower modulation, the modem uses the "LAPM, MNP or Buffer" error control sequence.

In another embodiment of the invention, a modem uses the data rate negotiated at the physical layer, rather than the modulation, to select the type of error control sequence. For example, if the modem connects at 2400 bits per second (bps) or below, the modem uses the "LAPM, MNP or Buffer" error control sequence. However, if the modem connects at a rate higher than 2400 bps, the modem uses the "LAPM or Disconnect" error control negotiation sequence. It should be noted that even though V.34 supports 2400 bps, I have observed that this data rate is unlikely to be used, i.e., a data rate of 2400 bps or less can be used to infer there is no high-speed modem in the data connection.

The above-described inventive concept provides a number of advantages. The user does not have to administer the modem to select a particular type of error control negotiation sequence via an AT command or other type of strap setting. Further, a modem incorporating the inventive concept still maintains compatibility with a large part of the currently installed-base of modems. Finally, this approach allows a high-speed modem to connect at the highest feasible rate and still negotiate the use of the LAPM protocol.

### BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram of a data communications equipment embodying the principles of the invention; and

FIG. 2 is a flow diagram of an illustrative method embodying the principles of the invention for use in the modem of FIG. 1.

### DETAILED DESCRIPTION

FIG. 1 shows an illustrative high-level block diagram of a modem embodying the principles of the invention. As

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shown, modem 100 couples to a communications channel (not shown) via line 133, which is, e.g., a local loop that couples modem 100 to a local central office (not shown). Modem 100 is also coupled to respective data terminal equipment (DTE) 10 via line 11. Other than the inventive concept, the components of modem 100 are well-known and will not be described in detail. Modem 100 includes DTE interface 105, microprocessor-based central processing unit (CPU) 110, memory 120 and digital signal processing circuitry (DSP) 130. Since FIG. 1 is a high-level block diagram, other parts of modem 100 not important to the inventive concept are assumed to be included within these representative components. For example, DSP 130 is representative of not only a digital signal processing chip, but also includes the "data access arrangement" (DAA) circuitry that couples any transmitted and received data signals to, and from, line 133. Further, although shown as single lines in FIG. 1, lines 11, 106, 111, 109, and 133, are representative of a plurality of signals as known in the art to interconnect the various components. For example, line 11 is representative of any one of a number of ways for coupling data communications equipment to data terminal equipment, e.g., a serial interface like that specified in Electronic Industry Association (EIA) standard RS-232.

As known in the art, CPU 110 provides a controlling function for modem 100, e.g., CPU 110 controls, via line 109, DSP 130 for establishing, maintaining, and disconnecting, from a data connection to a far-end modem (not shown), via line 106. In performing this controlling function, CPU 110 operates on, or executes, program data stored in memory 120 via line 111, which is representative of control, address, and data signals (not shown).

In accordance with the inventive concept, modem 100 dynamically selects the type of error control negotiation sequence as a function of the type of physical layer negotiated. Turning now to FIG. 2, an illustrative method embodying the principles of the invention will be described. The steps shown in FIG. 2 are illustratively stored in memory 120 as program data as represented by blocks 305, block 310, block 315, etc., of FIG. 1, respectively. For the purposes of this description, it is assumed that modem 100 has already initiated a data call to a far-end modem (not shown) and a handshaking sequence has begun. As known in the art, CPU 110 first negotiates with the far-end modem the physical layer of the data connection, as shown in step 305. (It should be realized that since this is a negotiation process, whether modem 100 is the originating, or answering, modem is irrelevant to the inventive concept). During the physical layer negotiation, modem 100 negotiates the type of modulation, e.g., V.22, V.22bis, V.32, V.32bis, and V.34 industry standards. After negotiation of the physical layer, CPU 110 evaluates a negotiated parameter of the physical layer in step 310. In particular, CPU 110 compares a value of the negotiated parameter to a predefined value. If the value of the negotiated parameter is greater than or equal to the predefined value, CPU 110 uses an "LAPM or Disconnect" error control negotiation sequence in step 315 as part of the link layer negotiation. The software instructions for executing the "LAPM or Disconnect" error control negotiation sequence are illustratively stored in memory 120 at location 121. With this negotiation setting, modem 100 tries for an extended length of time to negotiate a LAPM link layer on the data connection. If a LAPM link layer cannot be negotiated, modem 100 disconnects.

On the other hand, if the value of the negotiated parameter is less than the predefined value, CPU 110 uses an "LAPM, MNP or Buffer" error control negotiation sequence in step

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320 as part of the link layer negotiation. The software instructions for executing the "LAPM, MNP, or Buffer" error control negotiation sequence are illustratively stored in memory 120 at location 122. As described earlier, in this negotiation sequence modem 100 attempts to connect with the far-end modem for several seconds using an "LAPM" protocol like International Telecommunication Union (ITU) standard V.42. If the far-end modem does not appropriately respond, modem 100 then tries to connect with the far-end modem for several seconds using the "MNP" protocol. If this too is unsuccessful, modem 100 then falls back to a non-error control mode, i.e., the "Buffer" mode of operation.

In one embodiment of the invention, the negotiated parameter from the physical layer is the type of modulation negotiated in the physical layer. In particular, when modem 100 negotiates a V.32 or higher modulation, modem 100 performs step 315, described above. However, when modem 100 negotiates a V.22bis or lower modulation, modem 100 performs step 320, described above.

In another embodiment of the invention, the negotiated parameter from the physical layer is the negotiated data rate. For example, if modem connects below 4800 bps, modem 100 performs step 320, described above. However, when modem 100 connects at a rate equal to or higher than 4800 bps, modem 100 performs step 315, described above. It should be noted that even though high-speed modulations, like V.34, support rates below 4800, I have observed that these data rates are unlikely to be used. As a result, a data rate less than 4800 bps can be used to infer there is no high-speed modem in the data connection.

The above-described inventive concept provides a number of advantages. The user does not have to administer the modem to select a particular type of error control negotiation sequence for use during the link layer negotiation. Further, a modem incorporating the inventive concept still maintains compatibility with a large part of the currently installed-base of modems. Finally, this approach allows a high-speed modem to connect at the highest feasible rate and still negotiate the use of the LAPM protocol.

The foregoing merely illustrates the principles of the invention and it will thus be appreciated that those skilled in the art will be able to devise numerous alternative arrangements which, although not explicitly described herein, embody the principles of the invention and are within its spirit and scope.

For example, although the invention is illustrated herein as being implemented with discrete functional building blocks, e.g., a memory, CPU, etc., the functions of any one or more of those building blocks can be carried out using one or more appropriate integrated circuits, e.g., a microprocessor that includes memory.

In addition, although described in the context of a modem external to the data terminal equipment, the inventive concept applies to any other forms of coupling a modem to data terminal equipment, e.g., a modem that is internal to a personal computer or a modem that is part of a mobile phone transceiver. Finally, the selection of a link layer negotiation sequence can be a function of other data rates, types of modulations, and/or other parameters of the physical layer.

What is claimed:

1. A method for use in data communications equipment, the method comprising the steps of:

negotiating a physical layer of a data connection with a far-end data communications equipment to determine a set of parameters for the physical layer of the data connection with the far-end data communications equipment; and

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selecting one of a number of error control negotiation sequences as a function of a value of at least one parameter from the set of parameters for the physical layer.

2. The method of claim 1, further including the step of negotiating error control of the data connection with the far-end data communications equipment in accordance with the selected one of the number of error control negotiation sequences.

3. The method of claim 1, wherein the at least one parameter is the type of modulation negotiated with the far-end data communications equipment.

4. The method of claim 3, wherein the number of error control negotiation sequences include a Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence and a Link Access Protocol Modem or Disconnect sequence.

5. The method of claim 4, wherein the Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence is selected when the type of modulation negotiated is less than V32, and wherein the Link Access Protocol Modem or Disconnect sequence is selected when the type of modulation negotiated is greater than or equal to V32.

6. The method of claim 1, wherein the at least one parameter is the data rate negotiated with the far-end data communications equipment.

7. The method of claim 6, wherein the number of error control negotiation sequences include a Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence and a Link Access Protocol Modem or Disconnect sequence.

8. The method of claim 7, wherein the Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence is selected when the data rate is less than 4800 bits per second, and wherein the Link Access Protocol Modem or Disconnect sequence is selected the data rate is greater than or equal to 4800 bits per second.

9. Data communications apparatus comprising:

a memory that stores a number of error control negotiation sequences; and

processor circuitry that negotiates a physical layer of a data connection with a far-end data communications equipment to determine a set of parameters for the

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physical layer of the data connection with the far-end data communications equipment, and then selects from memory one of a number of error control negotiation sequences as a function of a value of at least one parameter from the set of parameters for the physical layer.

10. The apparatus of claim 9, wherein the processor negotiates error control of the data connection with the far-end data communications equipment in accordance with the selected one of the number of error control negotiation sequences.

11. The apparatus of claim 9, wherein the at least one parameter is the type of modulation negotiated with the far-end data communications equipment.

12. The apparatus of claim 11, wherein the number of error control negotiation sequences include a Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence and a Link Access Protocol Modem or Disconnect sequence.

13. The apparatus of claim 12, wherein the processor selects the Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence when the type of modulation negotiated is less than V32, and wherein the processor selects the Link Access Protocol Modem or Disconnect sequence when the type of modulation negotiated is greater than or equal to V32.

14. The apparatus of claim 9, wherein the at least one parameter is data rate negotiated with the far-end data communications equipment.

15. The apparatus of claim 9, wherein the number of error control negotiation sequences include a Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence and a Link Access Protocol Modem or Disconnect sequence.

16. The apparatus of claim 15, wherein the processor selects the Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence when the data rate is less than 4800 bits per second, and wherein the processor selects the Link Access Protocol Modem or Disconnect sequence when the data rate is greater than or equal to 4800 bits per second.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,710,761  
DATED : January 20, 1998  
INVENTOR(S) : Scott

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page of the patent, second column, six lines under the heading "ABSTRACT", change "type" to --types--.  
Column 2, line 27, after "at least two" change "type" to --types--.  
Column 4, line 22, change "4800" (in bold) to --4800-- (in regular font).  
Column 4, line 49, after "can be" delete "carded" and insert therefor --carried--.

Signed and Sealed this  
Twenty-sixth Day of May, 1998

Attest:



BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

## **Exhibit B**



US005778234A

**United States Patent** [19]

Hecht et al.

[11] Patent Number: **5,778,234**[45] Date of Patent: **Jul. 7, 1998****[54] METHOD FOR DOWNLOADING PROGRAMS**

[75] Inventors: **Gideon Hecht, Seminole; Kurt Ervin Holquist, Largo; Donald C. Snell, Clearwater, all of Fla.**

[73] Assignee: **Paradyne Corporation, Largo, Fla.**

[21] Appl. No.: **899,834**

[22] Filed: **Jul. 24, 1997**

**Related U.S. Application Data**

[62] Division of Ser. No. **880,237**, May 8, 1992.

[51] Int. CL<sup>6</sup> **G06F 9/44**

[52] U.S. CL. **395/712; 395/632**

[58] Field of Search **395/712, 651, 395/632**

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*Primary Examiner*—Emanuel Todd Voeltz

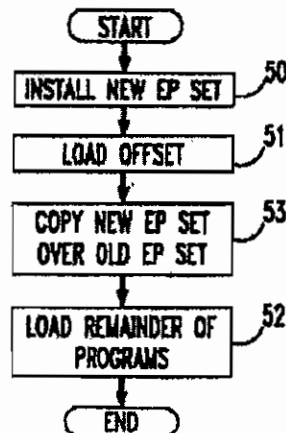
*Assistant Examiner*—Kakali Chaki

*Attorney, Agent, or Firm*—Thomas, Kayden, Horstemeier & Risley LLP

**[57] ABSTRACT**

A modified version of the operating communication program of a stored program controlled apparatus is downloaded by first downloading a segment of the new package of programs which contains the essential portion of the new programs. Control of the apparatus is then transferred to the new program segment. Thereafter, utilizing the downloaded essential portion of the new package of programs, the remainder of the new package of programs is downloaded.

**8 Claims, 1 Drawing Sheet**



U.S. Patent

Jul. 7, 1998

5,778,234

FIG. 1

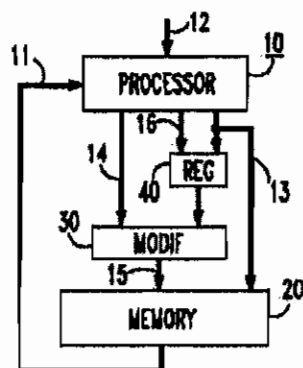


FIG. 2

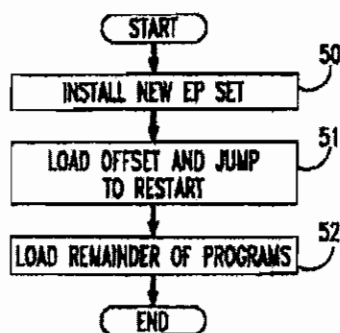
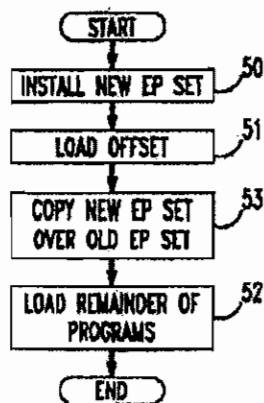


FIG. 3



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## METHOD FOR DOWNLOADING PROGRAMS

This application is a division of U.S. patent application having Ser. No. 07/880,257 of Hecht, et al., filed May 8, 1992.

### BACKGROUND OF THE INVENTION

This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of programs.

Stored program controlled apparatus can conveniently be divided into two types; one where the stored programs are completely unalterable under normal operating circumstances, and the other where the stored programs are alterable, at least at times, during normal operation. In apparatus of the first type, the program is often executed automatically and the user does not even know that the controlled apparatus is "stored program controlled". This is typically the case in equipment that is designed for people who are not knowledgeable in computers and for whom the equipment is just a tool of the trade. "Point of sale" terminals, such as check-out terminals at a supermarket, are a good example. Modems are another example. People who use this equipment desire fail-safe operation and they do not want to be bothered with loading programs, fixing program bugs, installing updated versions of software, etc.

One approach to programming such equipment is to imprint the program into read-only-memory integrated circuits and physically install the circuits into the equipment. The problem with this approach is that updated versions of the program require the creation of new sets of read-only memories and new installations.

When a communication link is present, "downloading" the programs to the equipment from a remote processor, through the communication link, forms another approach for programming the equipment. It has been known in the art for some time that it is feasible to download limited types of control information from a remote processor. It is also known to download entire machine language application programs. Often such equipment does not include writable non-volatile store, such as a hard disk, so the programs are stored in battery protected read/write memories.

This is an unattractive solution because it leaves a substantial portion of program memory to be at risk. To mitigate this problem, U.S. Pat. No. 4,724,521, suggests storing within read-only memories of the local equipment a number of general purpose routines which comprise instructions to be executed by the central processing unit to accomplish a particular program task. These, in effect, form a set of macro-instructions. The downloaded machine language program utilizes these macro-instructions to the extent possible, and thereby achieves flexibility without the need to download substantial amounts of program code.

In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents is not changed. That resident portion contains "boot-up" segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set. This set of programs should, of course, be a non-volatile store because there is always a possibility of power loss.

The fact that the EP set is needed to maintain communications presents a problem when the EP set itself needs to be

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modified or updated. Indeed, that is often the case with modems, where essentially the sole function of the modem software is to support communication.

### SUMMARY OF THE INVENTION

The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory. The start address specification means stores information that is downloaded through the communication link, and that information is used in defining the address from where the communication link programs are initiated.

In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address. Utilizing the most recently downloaded EP set of the new communication package, the second segment downloads the remainder of the new package.

### BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 presents a block diagram of an arrangement for carrying out this invention;

FIG. 2 is a flow diagram of a downloading process in accordance with this invention; and

FIG. 3 is a flow diagram of an augmented downloading process in accordance with this invention.

### DETAILED DESCRIPTION

A modem's primary function is to enable communications between a customer's digital equipment and a remote apparatus over a transmission medium. In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem. These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs—including the EP set of programs that carry out the elemental communications—are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile "boot-up" read-only-memory. All programs (including the boot-up programs) can be stored in a single memory arrangement which, for some applications, can consist of just two memory devices.

FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively. In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20. Modifier 30 is responsive to

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register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20. A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing.

It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory. It should also be understood, and noted, that although this invention is described in connection with modems, its principles are applicable to all stored program apparatus. In particular, the principles of this invention are applicable to all situations where it is desirable to download an entire set of new programs, including the EP set. For example, this invention is useful in PCs, "point of sale" terminals, etc.

The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30.

The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending information out on line 12 and for receiving information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere.

The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set.

In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP

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set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20.

After the new EP set is installed in memory locations X through X+N, where X is the offset address ( $X=M/2$ , for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address.

The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M).

It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Memory 20 must also be relatively fast because it directly affects the processing speed that can be attained with the FIG. 1 arrangement. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20. This memory must be erased in bulk before new information can be written in it. To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct chips (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves.

To summarize the downloading process of this invention,

1. Bulk erase the that half of memory 20 which does NOT contain the EP set of programs;
2. download a new EP set of programs to the erased half of memory 20;
3. download the offset address to pass control to the new EP set of programs;
4. bulk erase the other half of memory 20;
5. download the remainder of programs into memory 20.

If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can be manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10.

Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20):

1. Bulk erase the second half of memory 20;

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2. download a new EP set of programs to the second half of memory 20;
4. download the offset address to pass control to the new EP set of programs;
5. bulk erase the first half of memory 20;
6. copy the contents of the second half of memory 20 into the first half of memory 20;
7. reset the offset address to 0; and

8. download the remainder of programs into memory 20. 10  
Admittedly, during the copy sequence (which may also be a "move" sequence) the arrangement is vulnerable to power failures. Since the time of copying or moving is very small, this is a very unlikely event. Still, to protect against this unlikely event, the power source can be designed to have sufficient reserve to complete the copy operation, or to protect the starting address. A capacitor at the output of the power supply may supply the necessary power reserve.

In the arrangement described above where memory 20 consists of two FLASH EEPROM chips, register 40 needs to have only one bit of memory, and modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active.

We claim:

1. A method for installing a new set of communication programs  $P_{new}$  into a stored program controlled apparatus that includes a communication port and a memory by transmitting said set of programs  $P_{new}$  to said apparatus via said port, with the aid of a set of communications programs  $P_{old}$  already resident in said memory, where said set of programs  $P_{old}$  contains a subset of programs  $EP_{old}$  that occupy less than half of the memory and said set of programs  $P_{new}$  also contains a subset of programs  $EP_{new}$  that, when installed, occupy less than half of the memory, 35 comprising the steps of:

installing the  $EP_{new}$  programs in a first area of said memory that contains programs other than the  $EP_{old}$  programs, thereby overwriting at least a portion of one program in said  $P_{old}$  set of programs;

altering operation of said apparatus to execute the  $EP_{new}$  programs instead of the  $EP_{old}$  programs; and

installing the remaining programs of said  $P_{new}$  set of programs in a second area of said memory, said second area constituting memory locations not occupied by the  $EP_{new}$  programs. 40

2. The method of claim 1 further comprising

a step of moving, interposed between said step of altering operation of the apparatus and said step of installing the remaining programs, that installs said  $EP_{new}$  programs into memory locations starting at a location that corresponds to a starting location of the  $EP_{old}$  programs, and

a second step of altering operation of said apparatus to execute the  $EP_{new}$  programs in the installed locations by said step of moving. 45

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wherein said installing the remaining programs of said  $P_{new}$  set of programs stores the programs in memory locations not occupied with the  $EP_{new}$  programs installed by said step of moving.

3. The method of claim 1, further comprising the steps of: erasing said first area of said memory, said erasing step to be performed prior to said step of installing the  $EP_{new}$  programs into said first area of said memory; and

erasing said second area of said memory, said erasing step to be performed after said step of altering operation of the apparatus and prior to said step of installing the remaining programs of said  $P_{new}$  set of programs.

4. The method of claim 1, wherein said step of altering operation of said apparatus to execute said  $EP_{new}$  programs is accomplished by installing an offset address to pass control of said apparatus to said  $EP_{new}$  programs.

5. A method for installing a new set of communication programs  $P_{new}$  into a stored program controlled apparatus that includes a communication port and a memory by transmitting said set of programs  $P_{new}$  to said apparatus via said port, with the aid of a set of communications programs  $P_{old}$  already resident in said memory, where said set of programs  $P_{old}$  contains a subset of programs  $EP_{old}$  that occupy less than half of the memory and said set of programs  $P_{new}$  also contains a subset of programs  $EP_{new}$  that, when installed, occupy less than half of the memory, 50 comprising the steps of:

installing the  $EP_{new}$  programs in a first area of said memory that contains programs other than the  $EP_{old}$  programs, thereby overwriting at least a portion of one program in said  $P_{old}$  set of programs;

altering operation of said apparatus to execute the  $EP_{new}$  programs instead of the  $EP_{old}$  programs;

moving the  $EP_{new}$  programs from said first area of memory to a second area of said memory; and

installing the remaining programs of said  $P_{new}$  set of programs in said first area of memory. 55

6. The method of claim 5, further comprising the step of: erasing said first area of said memory, said erasing step to be performed prior to said step of installing the  $EP_{new}$  programs into said first area of said memory.

7. The method of claim 5, wherein said moving step further comprises the steps of:

copying the  $EP_{new}$  programs from said first area of memory to said second area of memory; and

erasing said first area of memory.

8. The method of claim 5, wherein said step of altering operation of said apparatus to execute said  $EP_{new}$  programs is accomplished by installing an offset address to pass control of said apparatus to said  $EP_{new}$  programs. 60

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,778,234  
DATED : July 7, 1998  
INVENTOR(S) : Hecht, *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 4, line 45, delete "that".

In column 5, line 48, insert ":" after "comprising".

In column 6, line 1, insert "step of" after the first appearance of "said" and before "installing".

Signed and Sealed this  
Seventeenth Day of November, 1998

Attest:



BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

## **Exhibit C**

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US006131159A

**United States Patent** [19]

Hecht et al.

[11] Patent Number: **6,131,159**[45] Date of Patent: **Oct. 10, 2000**[54] **SYSTEM FOR DOWNLOADING PROGRAMS**

[75] Inventors: **Gideon Hecht, Seminole; Kurt Ervin Holmquist, Largo; Donald C. Snell, Clearwater, all of Fla.**

[73] Assignee: **Paradyne Corporation, Largo, Fla.**

[21] Appl. No.: **07/880,257**

[22] Filed: **May 8, 1992**

[51] Int. Cl.<sup>7</sup> ..... **G06F 9/445**

[52] U.S. Cl. .... **713/1; 713/100; 711/1**

[58] Field of Search ..... **395/700, 651, 395/652, 653, 712; 364/DIG. 1, DIG. 2; 713/1, 2, 100; 711/114, 1, 145, 202-206; 710/23, 104**

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Primary Examiner—Thomas C. Lee

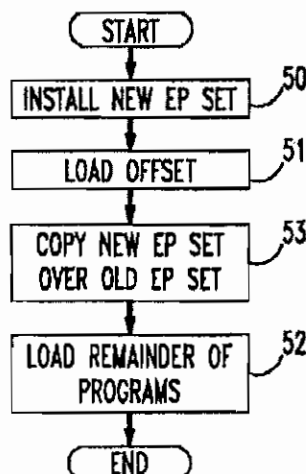
Assistant Examiner—Rijue Mai

Attorney, Agent, or Firm—Thomas, Kayden, Horstemeier & Risley LLP

[57] **ABSTRACT**

A modified version of the operating communication program of a stored program controlled apparatus is installed with the aid of a downloadable start address specification means, optionally realized with an EEPROM memory. The start address specification means stores information that is downloaded through a communication port in the apparatus, and that information is used in defining the address from where the communication programs are initiated. In accordance with the method of this invention, downloading of the entire new set of programs is effected by first downloading a segment of the essential portion of the new package of programs. Control is then transferred to the new segment by downloading appropriate information into the start address specification means. Thereafter, utilizing the downloaded essential portion of the new package of programs, the remainder of the new package is downloaded.

21 Claims, 1 Drawing Sheet



U.S. Patent

Oct. 10, 2000

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FIG. 1

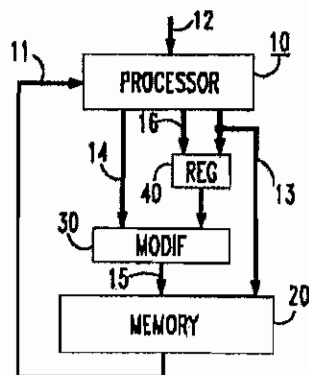


FIG. 2

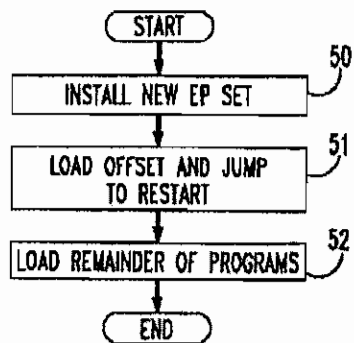
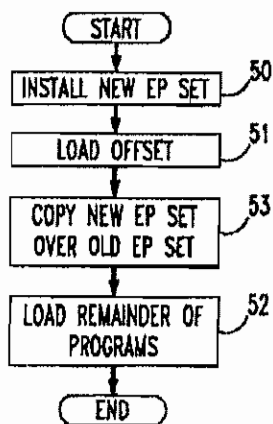


FIG. 3



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## SYSTEM FOR DOWNLOADING PROGRAMS

### BACKGROUND OF THE INVENTION

This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of programs.

Stored program controlled apparatus can conveniently be divided into two types; one where the stored programs are completely unalterable under normal operating circumstances, and the other where the stored programs are alterable, at least at times, during normal operation. In apparatus of the first type, the program is often executed automatically and the user does not even know that the controlled apparatus is "stored program controlled". This is typically the case in equipment that is designed for people who are not knowledgeable in computers and for whom the equipment is just a tool of the trade. "Point of sale" terminals, such as check-out terminals at a supermarket, are a good example. Modems are another example. People who use this equipment desire fail-safe operation and they do not want to be bothered with loading programs, fixing program bugs, installing updated versions of software, etc.

One approach to programming such equipment is to imprint the program into read-only-memory integrated circuits and physically install the circuits into the equipment. The problem with this approach is that updated versions of the program require the creation of new sets of read-only memories and new installations.

When a communication link is present, "downloading" the programs to the equipment from a remote processor, through the communication link, forms another approach for programming the equipment. It has been known in the art for some time that it is feasible to download limited types of control information from a remote processor. It is also known to download entire machine language application programs. Often such equipment does not include writable non-volatile store, such as a hard disk, so the programs are stored in battery protected read/write memories. This is an unattractive solution because it leaves a substantial portion of program memory to be at risk. To mitigate this problem, U.S. Pat. No. 4,724,521, suggests storing within read-only memories of the local equipment a number of general purpose routines which comprise instructions to be executed by the central processing unit to accomplish a particular program task. These, in effect, form a set of macro-instructions. The downloaded machine language program utilizes these macro-instructions to the extent possible, and thereby achieves flexibility without the need to download substantial amounts of program code.

In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents are not changed. That resident portion contains "boot-up" segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set. This set of programs should, of course, be a non-volatile store because there is always a possibility of power loss.

The fact that the EP set is needed to maintain communications presents a problem when the EP set itself needs to be modified or updated. Indeed, that is often the case with modems, where essentially the sole function of the modem software is to support communication.

### SUMMARY OF THE INVENTION

The problem of downloading a modified version of the operating communication program, and the problem of

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effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory. The start address specification means stores information that is downloaded through the communication link, and that information is used in defining the address from where the communication link programs are initiated.

In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address. Utilizing the most recently downloaded EP set of the new communication package, the second segment downloads the remainder of the new package.

### BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 presents a block diagram of an arrangement for carrying out this invention;

FIG. 2 is a flow diagram of a downloading process in accordance with this invention; and

FIG. 3 is a flow diagram of an augmented downloading process in accordance with this invention.

### DETAILED DESCRIPTION

A modem's primary function is to enable communications between a customer's digital equipment and a remote apparatus over a transmission medium. In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem. These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs—including the EP set of programs that carry out the elemental communications—are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile "boot-up" read-only-memory. All programs (including the boot-up programs) can be stored in a single memory arrangement which, for some applications, can consist of just two memory blocks.

FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively. In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 13 supplying the address information to memory 20. Modifier 30 is responsive to register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20. A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing.

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It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory. It should also be understood, and noted, that although this invention is described in connection with modems, its principles are applicable to all stored program apparatus. In particular, the principles of this invention are applicable to all situations where it is desirable to download an entire set of new programs, including the EP set. For example, this invention is useful in PCs, "point of sale" terminals, etc.

The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30.

The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending information out on line 12 and for receiving information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere.

The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set.

In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20.

After the new EP set is installed in memory locations X through X+N, where X is the offset address ( $X=M/2$ , for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is

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found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address.

The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M).

It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20. This memory must be erased in bulk before new information can be written in it. To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves.

To summarize the downloading process of this invention,

1. Bulk erase the first half of memory 20 which does NOT contain the EP set of programs;
2. download a new EP set of programs to the erased half of memory 20;
3. download the offset address to pass control to the new EP set of programs;
4. bulk erase the other half of memory 20;
5. download the remainder of programs into memory 20.

If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can be manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10.

Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20):

1. Bulk erase the second half of memory 20;
2. download a new EP set of programs to the second half of memory 20;
3. download the offset address to pass control to the new EP set of programs;
4. bulk erase the first half of memory 20;
5. copy the contents of the second half of memory 20 into the first half of memory 20;
6. reset the offset address to 0; and
8. download the remainder of programs into memory 20.

Admittedly, during the copy sequence (which may also be a "move" sequence) the arrangement is vulnerable to power failures. Since the time of copying or moving is very small, this is a very unlikely event. Still, to protect against this unlikely event, the power source can be designed to have sufficient reserve to complete the copy operation, or to protect the starting address. A capacitor at the output of the power supply may supply the necessary power reserve.

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In the arrangement described above where memory 20 consists of two FLASH EEPROM chips, register 40 needs to have only one bit of memory, and modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active.

What is claimed is:

1. A system comprising:

(a) a processor;

(b) a memory, and a set of programs stored in said memory that are executed when the system needs to be initialized, said memory being of a type which may be completely updated in its entirety but which is not volatile, said memory being the only program memory in said system; and

(c) alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing.

2. The system of claim 1 wherein said memory is an EEPROM memory.

3. The system of claim 1 wherein said memory consists of 2-FLASH EEPROM devices.

4. The system of claim 1 wherein said alterable storage means is an EEPROM memory.

5. The system of claim 1 further comprising translation means interposed between said alterable storage means and said memory, wherein said alterable storage means holds an address that translates between addresses directed to the memory via said translation means and addresses actually applied to the memory by said translation means.

6. A system comprising:

(a) a processor;

(b) a memory coupled to said processor, said memory being the only program memory in the system, said memory being completely updatable in its entirety but non-volatile, there being a set of programs stored in said memory that are executed when the system needs to be initialized; and

(c) alterable memory means for storing a multi-bit memory address that controls the starting address accessed by the processor when initializing.

7. The system of claim 6 further comprising means for receiving a trigger signal at a telecommunications input port of the system to begin execution of said programs.

8. A system comprising:

(a) a processor;

(b) a memory and a communications port coupled to said processor, said communications port being adapted to communicate with devices which are external to said system, said memory being completely updatable in its entirety but non-volatile;

(c) a program module in said memory that, when activated by said processor, effects communication with said port; and

(d) operationally alterable means for setting the starting address of said program, which address is supplied to said system via said communication port.

9. The system of claim 8 wherein:

(a) said memory contains a first set of programs and a second set of programs;

(b) said memory is at least twice the size of the size of the first set of programs; and

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(c) said operationally alterable means sets the starting position of the program executed by said processor in connection with communication with said port at a second specified location that is M removed from the first location, M being half the size of said memory.

10. A system comprising:

(a) a processor;

(b) a communication port coupled to said processor, said communication port being adapted to communicate with devices which are external to said system;

(c) a memory coupled to said processor, said memory being non-volatile and capable of being completely updated in its entirety, said memory containing programs, including a set of programs that are executed when the system needs to be initialized and a program for controlling communication through said communication port; and

(d) means for activating said program for controlling communication and receiving information through said communication port to modify the programs in said memory, said information including the program for controlling communication through said communication port and a command that is executed by said processor effectively when it is received.

11. The system of claim 10 wherein the communication port is a telecommunication port.

12. The system of claim 10 wherein the communication port is a telecommunication port and the programs execute the functions of a modem.

13. The system of claim 10 where the communication port receives commands to be executed by the processor and data to be stored in the memory.

14. The system of claim 10 wherein said means for receiving includes means for altering the program according to the information obtained by the means for receiving.

15. The system of claim 10 wherein said means for receiving modifies the programs by altering a portion of the memory contents pursuant to data received via said communication port.

16. The system of claim 10 wherein said means for receiving modifies the programs by replacing them with program data received via said communication port.

17. The system of claim 10 where the means for altering alters all of the programs in the system in a single communication session with said communication port.

18. A system comprising:

(a) a processor;

(b) a memory coupled to said processor, said memory being of a type, which is completely updatable in its entirety but non-volatile;

(c) a set of program means stored in said memory that are activated when said system needs to be updated with a new set of programs, and

(d) alterable storage means for holding an offset memory address that is used to point to a starting address accessed by said processor when initializing.

19. The system of claim 18 wherein said memory is an EEPROM memory.

20. The system of claim 18 wherein said memory consists of 2 FLASH EEPROM devices.

21. The system of claim 18 wherein said alterable storage means is an EEPROM memory.

\* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,131,159  
DATED : October 10, 2000  
INVENTOR(S) : Hecht, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

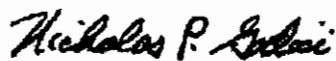
Column 4, line 40, insert "be" between "can" and "manufactured".

Column 6, line 49, delete "," after "type".

Column 6, line 52, change "wit" to --with--.

Signed and Sealed this  
Twenty-fourth Day of April, 2001

Attest:



NICHOLAS P. CODICI

Attesting Officer

Acting Director of the United States Patent and Trademark Office

## **Exhibit D**



US006950444B1

(12) **United States Patent**  
Holmquist et al.

(10) Patent No.: **US 6,950,444 B1**  
(45) Date of Patent: **Sep. 27, 2005**

(54) **SYSTEM AND METHOD FOR A ROBUST PREAMBLE AND TRANSMISSION DELIMITING IN A SWITCHED-CARRIER TRANSCEIVER**

5,822,373 A • 10/1998 Addy ..... 375/259  
6,252,865 B1 • 6/2001 Walton et al. .... 370/335  
6,353,635 B1 • 3/2002 Montague et al. .... 375/240,26  
6,651,210 B1 • 11/2003 Trott et al. .... 714/758

• cited by examiner

(75) Inventors: Kurt Holmquist, Largo, FL (US);  
Joseph Chapman, Seminole, FL (US)

Primary Examiner—Kenneth Vanderpuye  
(74) Attorney, Agent, or Firm—Thomas, Kayden,  
Horstemeyer & Risley LLP

(73) Assignee: Paradyne Corporation, Largo, FL  
(US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 812 days.

# (57) ABSTRACT

A method and system for robust delimiting of transmitted messages in switched-carrier operation in which a preamble precedes each communication message with the preamble comprising symbols transmitted at a rate lower than that of the following data. The lower rate symbols of the preamble significantly increase the probability that the decoder will decode the preamble symbols error free. Communication line control information can be included in the robust preamble, thereby ensuring that line control information is reliably transferred over the communication channel. The first symbol of the preamble can be transmitted at the lower symbol rate and at an increased power level, thereby clearly and reliably delimiting the beginning of a transmission. The end of the communication message can be reliably delimited by sending the first symbol containing only bits from a next cell of information at a lower symbol rate and including an extra bit in that symbol. The extra bit can be set to indicate to a receiver whether the last cell of information has just begun.

(21) Appl. No.: 09/637,185

(22) Filed: Aug. 11, 2000

## Related U.S. Application Data

(60) Provisional application No. 60/150,436, filed on Aug. 24, 1999.

(51) Int. Cl.<sup>7</sup> ..... H04L 12/56

(52) U.S. Cl. .... 370/476; 370/477

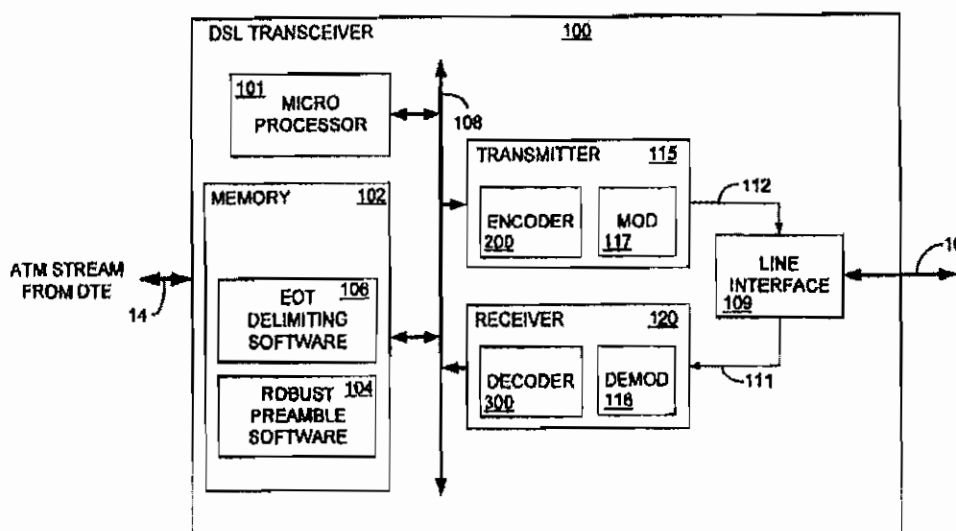
(58) Field of Search ..... 370/476, 471,  
370/472, 474, 477, 389

## (56) References Cited

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5,535,199 A • 7/1996 Amri et al.

55 Claims, 10 Drawing Sheets



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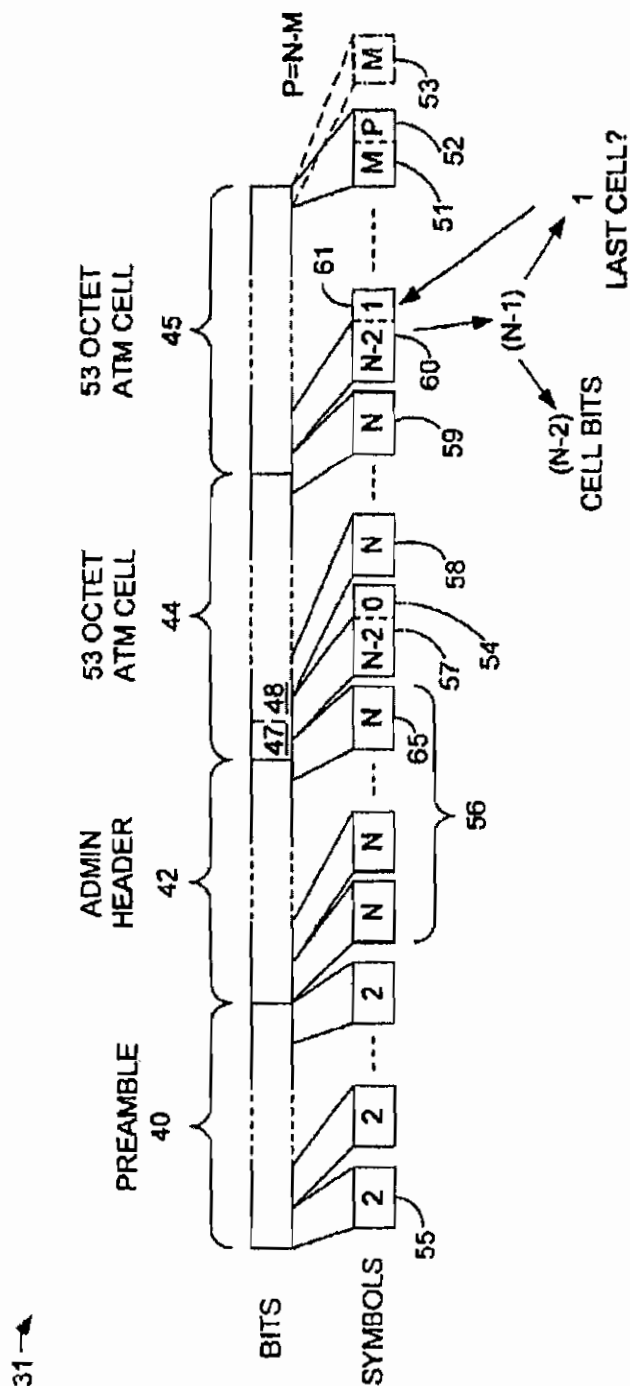


FIG. 3A

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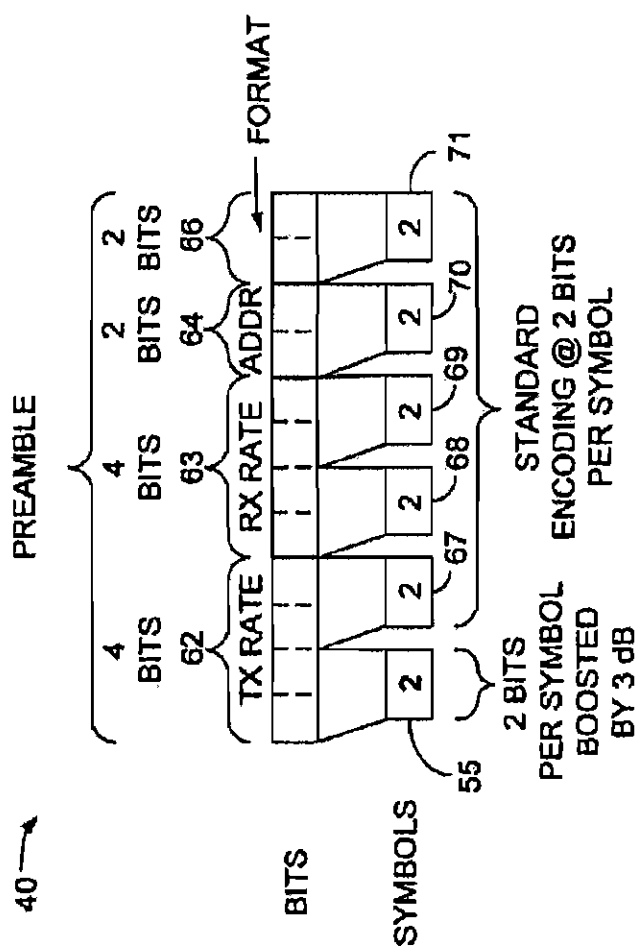


FIG. 3B

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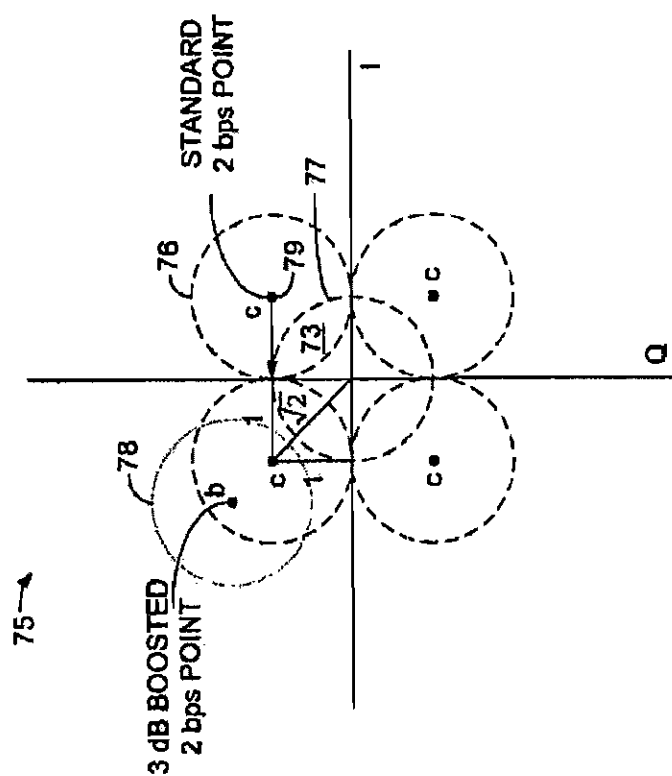


FIG. 4A

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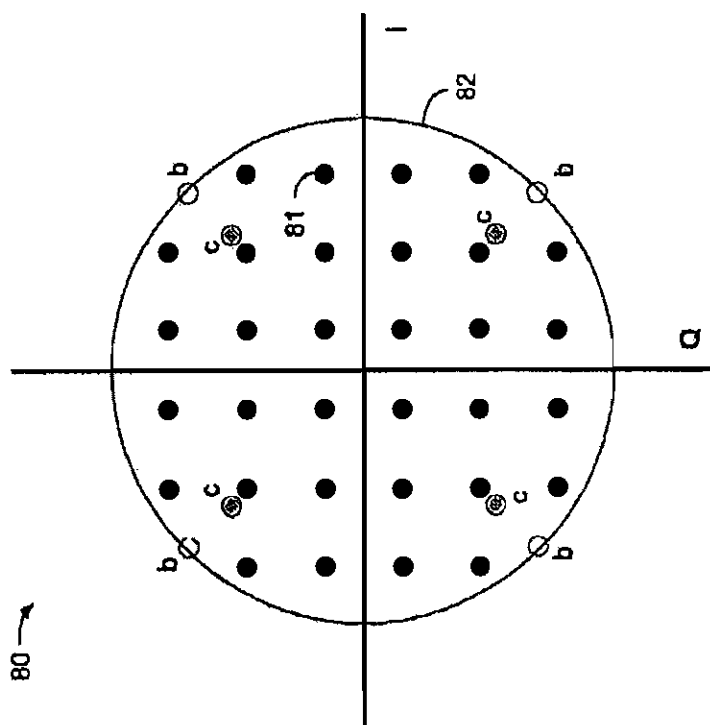
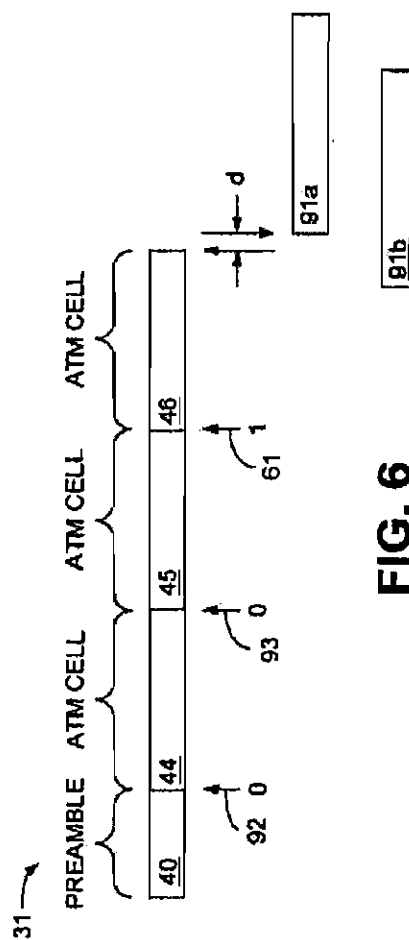
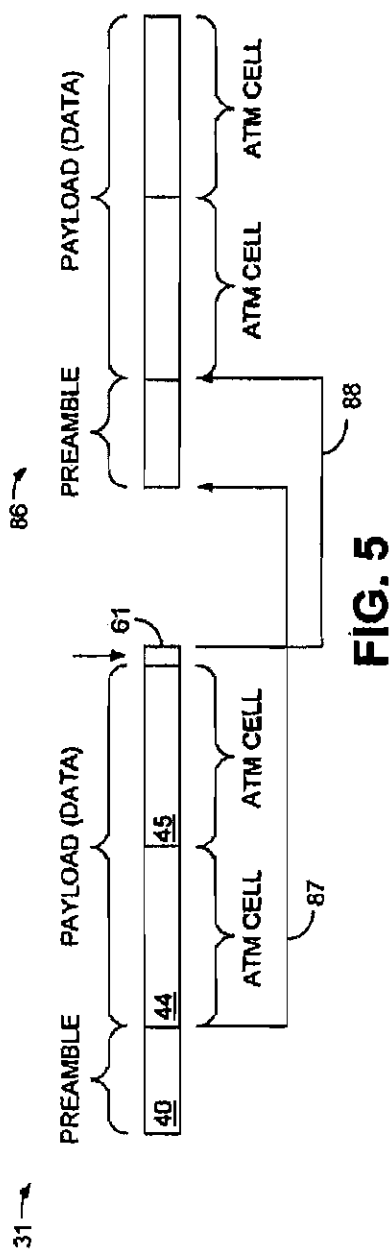


FIG. 4B



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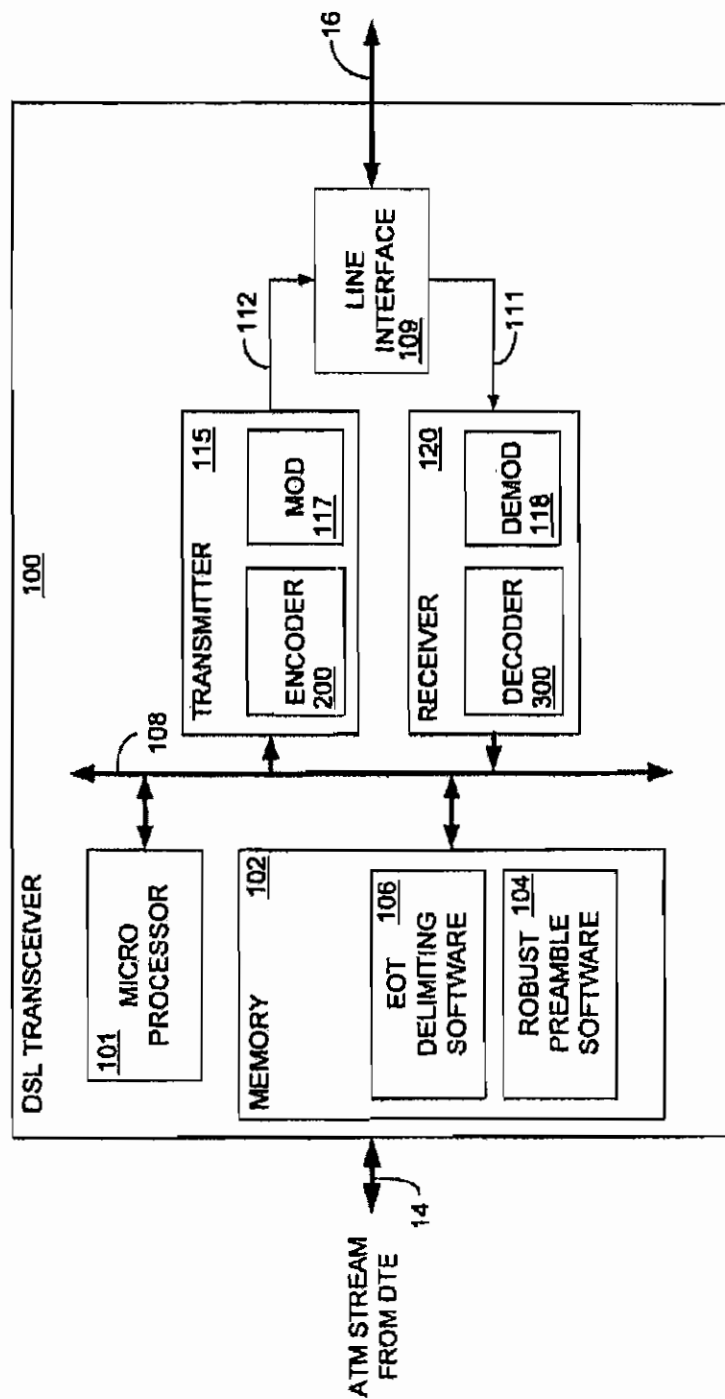


FIG. 7

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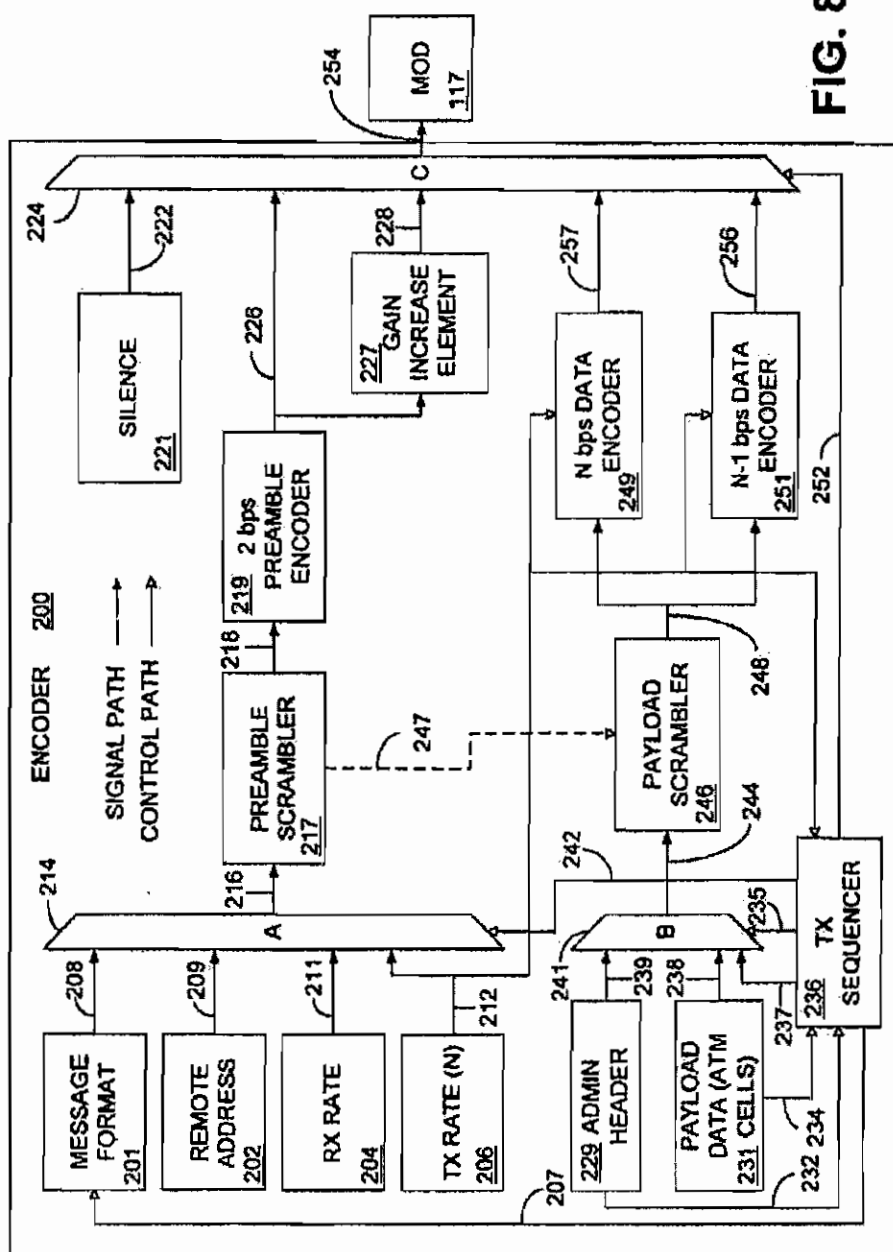


FIG. 8

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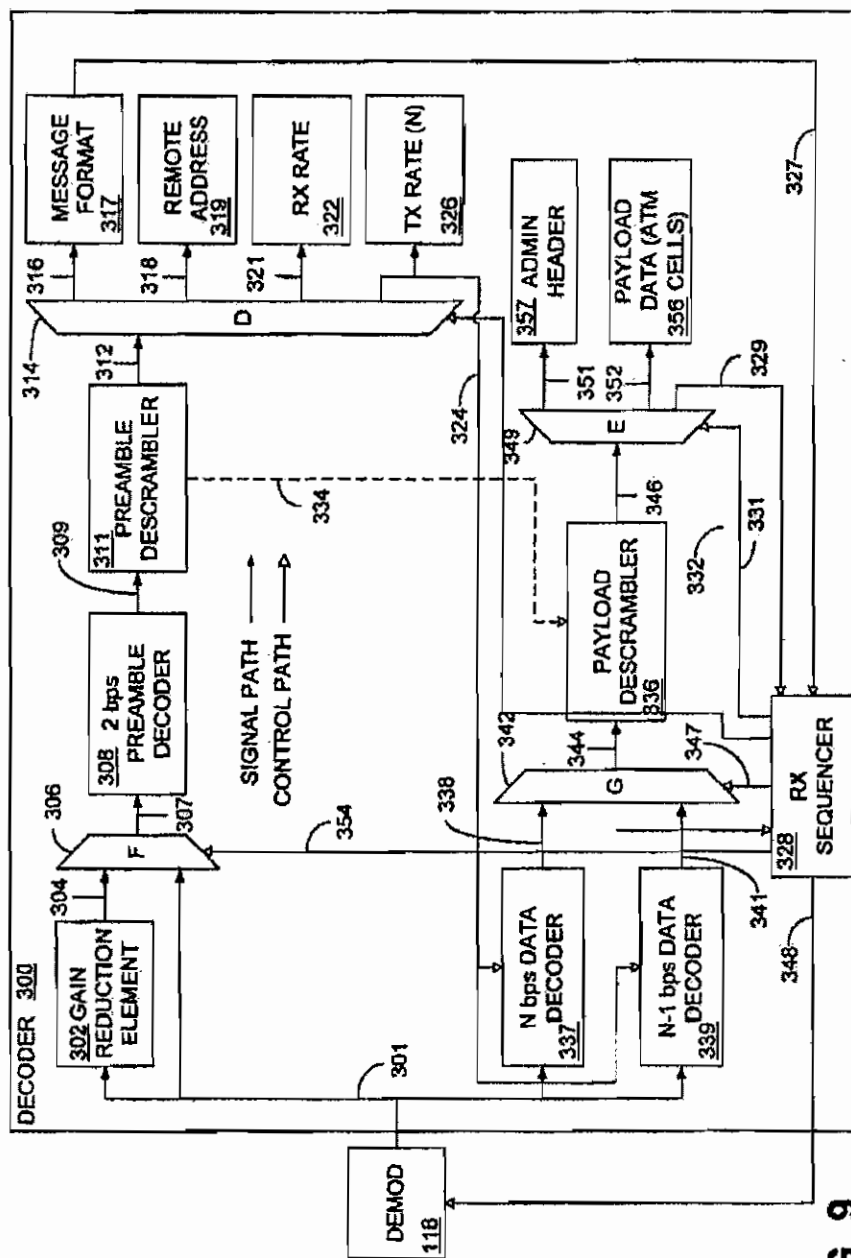


FIG. 9

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# SYSTEM AND METHOD FOR A ROBUST PREAMBLE AND TRANSMISSION DELIMITING IN A SWITCHED-CARRIER TRANSCIVER

## CROSS-REFERENCE TO RELATED APPLICATIONS

This document claims priority to, and the benefit of, the filing date of Provisional Application Ser. No. 60/150,436 entitled "A TECHNIQUE FOR ROBUST SIGNAL DELIMITING AND ENCODING OF CRITICAL LINK CONTROL SIGNALS APPLIED TO TRANSMISSION OF ATM CELLS OVER A DSL USING ADAPTIVE TIME DOMAIN DUPLEX (ATDD)," filed on Aug. 24, 1999, which is hereby incorporated by reference.

## TECHNICAL FIELD

The present invention relates generally to communications systems, and more particularly, to a system and method for a robust preamble and transmission delimiting in a switched-carrier transceiver.

## BACKGROUND OF THE INVENTION

Data communication typically occurs as the transfer of information from one communication device to another. This is typically accomplished by the use of a modem located at each communication endpoint. In the past, the term modem denoted a piece of communication apparatus that performed a modulation and demodulation function, hence the term "modem". Today, the term modem is typically used to denote any piece of communication apparatus that enables the transfer of data and voice information from one location to another. For example, modem communication systems use many different technologies to perform the transfer of information from one location to another. Digital subscriber line (DSL) technology is one vehicle for such transfer of information. DSL technology uses the widely available subscriber loop, the copper wire pair that extends from a telephone company central office to a residential location, over which communication services, including the exchange of voice and data, may be provisioned. DSL devices can be referred to as modems, or, more accurately, transceivers, which connect the telephone company central office to the user, or remote location typically, referred to as the customer premises. DSL communication devices utilize different types of modulation schemes and achieve widely varying communication rates. However, even the slowest DSL communications devices achieve data rates far in excess of conventional point-to-point modems.

DSL transceivers can be used to provision a variety of communication services using, for example, asynchronous transfer mode (ATM). ATM defines a communication protocol in which 53 octet (byte) cells are used to carry information over the DSL communication channel. The first five octets of the ATM cell are typically used for overhead and the remaining 48 octets are used to carry payload data. When using a switched-carrier transmission methodology, a control transceiver may be connected via the DSL to one or more remote transceivers. In such a communication scheme, the transmission is commonly referred to as "half-duplex," which is defined as two way electronic communication that takes place in only one direction at a time. With only a single remote transceiver on a line, switched-carrier transmission may instead be employed in full-duplex mode (i.e., allowing transmission in both directions simultaneously). In this case, full-duplex operation is typically enabled by employing

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either echo cancellation or frequency division multiplexing. Hybrid techniques are possible such as one in which there are multiple remote transceivers and communication takes place between the control transceiver and only one remote transceiver in full-duplex fashion. As it relates to the present invention, the common characteristic of these communication techniques is the use of a switched-carrier modulation in which transmitters are deliberately silent for some interval between signal transmissions. For simplicity, the following discussions assume the simplest case of using switch carrier modulation with a half-duplex (also sometimes referred to as "time domain duplex") line usage discipline.

Before the transmission of ATM cells, a preamble containing channel, transmission, address and administrative information may be transmitted by the transceiver. The application of this preamble is sometimes referred to as "framing" the data to be transmitted. Due to the switched-carrier nature of the transmission, silence precedes this preamble and it is of course important for all symbols in this preamble to be received error free. It is also desirable to have the ability to precisely delimit the beginning and end of a transmission to within one transmitted symbol interval. Robustly delimiting the beginning of a message enables a receiving transceiver to reliably begin immediately decoding the message at the correct symbol. Likewise, robustly delimiting the end of a message enables a receiving transceiver to reliably decode the entire message through the final symbol and then stopping so as to prevent data loss and to prevent the inclusion of any false data. Furthermore, by communicating the end of message indicator to a receiving transceiver prior to the actual end of the message, line turnaround time (i.e., idle time on the line between transmissions) can be reduced, thereby increasing the effective use of the available line bandwidth.

Because the most efficient signal constellation encoding cannot allocate signal space to silence, it is impractical to reliably discriminate silence from a signal when analyzing only a single symbol encoding an arbitrary data value.

To improve message delimiting, existing techniques use special marker symbols whose symbol indices are greater than those used to encode data. At N bits per symbol (bps) data is encoded using symbol indices 0 through  $2^N-1$ . The special symbols use indices  $2^N$  and above. While these special marker symbols are useful for marking the beginning and end of a transmission, their placement at the outer edges of a constellation raises the peak signal, thus increasing the peak to average ratio (PAR) across all data rates by as much as 4 dB. Unfortunately, discrimination of special symbols has the same error threshold as does decoding of data.

Thus, it would be desirable to have a robust manner in which to detect the beginning and end of a transmission so that line bandwidth can be most efficiently allocated. Furthermore, it would be desirable to robustly transmit a message preamble including control information thereby greatly improving the probability that the preamble is received error free.

## SUMMARY OF THE INVENTION

The present invention provides an improved system and method for robustly delimiting a message transmission in switched-carrier communication systems. The invention provides a method and system for transmission of a message preamble in which transmission of the preamble is more robust than the data. In this manner, the beginning and end of a transmission can be robustly delimited and channel control information can be reliably conveyed to a receiving transceiver.

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The system of the present invention uses a novel header application, which enables the transport of ATM, or any other data, efficiently and economically over a communications channel, such as a DSL communications channel.

Briefly described, in architecture, the system for robust transmission delimiting comprises a communication message including a preamble including a plurality of bits representing communication link control information, and an encoder configured to encode the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel.

In another aspect, the invention is a system for delimiting the end of a transmission. The system takes a communication message segmented into a plurality of fixed size units, each fixed size unit including a plurality of bits, and includes an encoder configured to encode the plurality of bits into a plurality of symbol indices at a first data rate. The encoder is also configured to encode the first symbol index containing only bits from each fixed size unit at a data rate lower than that of the first data rate.

The present invention can also be viewed as a method for robust transmission delimiting comprising the steps of applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information, and encoding the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

In another aspect, the invention is a method for delimiting the end of a transmission comprising the steps of segmenting a communication message into a plurality of fixed size units, each unit including a plurality of bits, encoding a plurality of the bits in the units into a plurality of symbol indices, the symbol indices being encoded at a first rate, and encoding the first symbol index containing only bits from each fixed size unit at a rate lower than that of the first rate.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The invention can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present invention. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

FIG. 1 is a schematic view illustrating a switched-carrier half-duplex communication environment, in which DSL transceivers containing the present invention reside;

FIG. 2A is an illustration of the time-domain duplex communication methodology employed by the DSL transceivers of FIG. 1;

FIG. 2B is a schematic view illustrating, in further detail, a communication message of FIG. 2A;

FIG. 3A is a schematic view illustrating the bit to symbol relationship of the communication message of FIG. 2B;

FIG. 3B is a schematic view illustrating, in further detail, the preamble of FIG. 3A;

FIG. 4A is a graphical illustration representing a two (2) bit per symbol signal space constellation and the increased energy symbol of FIG. 3B;

FIG. 4B is a graphical illustration showing an exemplar grouping of constellation points representing different bit per symbol rates in accordance with an aspect of the invention;

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FIG. 5 is a schematic view illustrating the communication message of FIG. 3A and a technique for scrambling that further improves reliable transmission of the message preamble;

FIG. 6 is a schematic view illustrating the communication message of FIG. 3A and the reduced line turn around delay made possible by an aspect of the invention;

FIG. 7 is a block diagram illustrating the control DSL transceiver of FIG. 1;

FIG. 8 is a block diagram illustrating the encoder of FIG. 7; and

FIG. 9 is a block diagram illustrating the decoder of FIG. 7.

#### DETAILED DESCRIPTION OF THE INVENTION

Although, described with particular reference to the transmission of ATM cells over a DSL communication channel, the system and method for a robust preamble and transmission delimiting can be implemented to transmit all forms of data in any switched-carrier transmission system in which it is desirable to send a robust preamble and to robustly delimit the beginning and end of each communication message.

Furthermore, the system and method for a robust preamble and transmission delimiting can be implemented in software, hardware, or a combination thereof. In a preferred embodiment(s), selected portions of the system and method for a robust preamble and transmission delimiting are implemented in hardware and software. The hardware portion of the invention can be implemented using specialized hardware logic. The software portion can be stored in a memory and be executed by a suitable instruction execution system (microprocessor). The hardware implementation of the system and method for a robust preamble and transmission delimiting can include any or a combination of the following technologies, which are all well known in the art: an discrete logic circuit(s) having logic gates for implementing logic functions upon data signals, an application specific integrated circuit having appropriate logic gates, a programmable gate array(s) (PGA), a field programmable gate array (FPGA), etc.

Furthermore, the robust preamble and transmission delimiting software, which comprises an ordered listing of executable instructions for implementing logical functions, can be embodied in any computer-readable medium. Moreover, use by or in connection with an instruction execution system, apparatus, or device, such as a computer-based system, processor-containing system, or other system that can fetch the instructions from the instruction execution system, apparatus, or device and execute the instructions.

In the context of this document, a "computer-readable medium" can be any means that can contain, store, communicate, propagate, or transport the program for use by or in connection with the instruction execution system, apparatus, or device. The computer readable medium can be, for example but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, device, or propagation medium. More specific examples (a non-exhaustive list) of the computer-readable medium would include the following: a electrical connection (electronic) having one or more wires, a portable computer diskette (magnetic), a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory) (magnetic), an optical fiber (optical), and a portable compact disc read-only memory (CDROM) (optical). Note that the computer-

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readable medium could even be paper or another suitable medium upon which the program is printed. As the program can be electronically captured, via for instance optical scanning of the paper or other medium, then compiled, interpreted or otherwise processed in a suitable manner if necessary, and then stored in a computer memory.

Turning now to the drawings, FIG. 1 is a schematic view illustrating a switched-carrier half-duplex communication environment 1, in which DSL transceivers containing the present invention reside. Although the invention will be described below in a half-duplex communication environment, the DSL transceivers containing the invention may be used in a switched-carrier full-duplex environment as well. In such a case, full-duplex operation may be enabled using technologies such as echo cancellation or frequency division multiplexing. Communication environment 1, includes central office 12 connected via communication channel 16 to customer premises 21. Communication channel 16 can be any physical medium over which communications signals can be exchanged, and in the preferred embodiment, is the copper wire pair that extends from a telephone company central office to an end-user location, such as a home or office. Central office 12 includes DSL transceiver 100 connected to communication channel 16. DSL transceiver 100 processes data via connection 14. DSL transceiver 100 exchanges data via connection 14 with any data terminal equipment (DTE), such as a computer or data terminal.

Customer premises 21 includes one or more DSL transceivers 150 connected via internal infrastructure wiring 18 to communication channel 16. The infrastructure wiring 18 can be, for example but not limited to, the telephone wiring within a private residence or within an office. DSL transceivers 150 can be connected to a variety of telecommunication devices located at customer premises 21. For example, DSL transceiver 150 connects via connection 22 to a personal computer 26. Although additional DSL transceivers can be located at customer premises 21, an exemplar one of which is indicated using reference numeral 155, the aspects of the invention to be discussed below are also applicable if only one DSL transceiver 150 is located at customer premises 21. In the example given in FIG. 1, DSL transceiver 155 connects to computer 28 via connection 29.

The DSL transceiver 100 located at central office 12 is considered a "control device" and the DSL transceiver 150 located at customer premises 21 is considered a "remote device." This is so because the control DSL transceiver 100 controls the communication sessions by periodically polling each remote DSL transceiver 150 to determine whether the remote device has information to transmit. Regardless of the number of DSL transceivers located at customer premises 21, the method of communication between DSL transceiver 100 located at central office 12 and DSL transceiver 150 located at customer premises 21 is half-duplex in nature, sometimes referred to as adaptive time-domain duplex, or data driven half-duplex, unless the above-mentioned technologies such as echo cancellation or frequency division multiplexing allow full-duplex operation between the control transceiver 100 and one remote transceiver 150. This means that during any time period only one DSL transceiver may transmit at any time. In the situation in which there are multiple DSL transceivers located at customer premises 21, the DSL transceiver 100 located at central office 12 periodically polls each DSL transceiver located at customer premises 21 at an appropriate time to determine whether any of the remotely located DSL transceivers have any information to transmit to central office 12. If only one DSL

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transceiver 150 is located at customer premises 21, the communication method may be half-duplex in nature or conventional full-duplex techniques may be used (e.g., using either frequency division multiplexing or echo cancellation).

FIG. 2A is a schematic view illustrating the time-domain duplex communication methodology between a control DSL transceiver 100 and a remote DSL transceiver 150. When a control DSL transceiver 100 desires to send a message to a remote DSL transceiver 150 the control DSL transceiver 100 sends a communication message 31 including a preamble and any information that is to be transmitted. There are times when the communication message may include only a preamble. After the transmission of communication message 31, the remote DSL transceiver to which communication message 31 is addressed (in this example remote DSL transceiver 150) responds with communication message 32. After the remote DSL transceiver 150 completes the transmission of communication message 32, the control DSL transceiver 100 is now free to send another communication message 34 to either the same remote DSL transceiver 150 or, if present, a different remote DSL transceiver, such as DSL transceiver 155 (remote "n") of FIG. 1. As illustrated in FIG. 2A, remote DSL transceiver "n" responds with communication message 36. In this manner, the communication methodology between control DSL transceiver 100 and all remote DSL transceivers 150, 155, . . . n, is switched-carrier and time-domain duplexed.

FIG. 2B is a schematic view illustrating, in further detail, the communication message 31 of FIG. 2A. Communication message 31 begins with preamble 40 followed by optional administrative header 42. In accordance with an aspect of the invention, all communication messages, regardless of the content, begin with preamble 40. Administrative header 42 is optional and can be used to send information that is neither part of the preamble 40 or of any data to follow. For example, the administrative header 42 could convey a description of noise level conditions at one end so the other end may opt to increase or reduce the power level of its transmission as necessary. Likewise, the administrative header 42 sent by a remote transceiver could contain information regarding the amount of payload information that the remote transceiver is ready to transmit and its relative priorities so that the control transceiver could alter the amount of time that this remote transceiver is given to transmit its data (relative to any other transceivers connected to the line). When the payload data comprises ATM cells, the control transceiver could use messages conveyed by the administrative header 42 to direct remote devices to activate or deactivate various ATM virtual circuits.

If data is included in communication message 31, one or more ATM cells follow the optional administrative header 42. Although illustrated using three ATM cells, 44, 45 and 46, there are situations in which no ATM cells, or for that matter, no information of any kind, follows preamble 40. In the case in which information does follow preamble 40, and for purposes of illustration only, ATM cells 44, 45 and 46 are each standard 53 octet ATM cells. For example, ATM cell 44 includes 5 octet ATM header 47 and 48 octets of ATM data 48. ATM cells 45 and 46 are identical in structure to ATM cell 44. ATM cells 44, 45 and 46 adhere to the conventional ATM cell structure as defined in standardized ATM literature. It should be noted that optional administrative header 42 does not follow the standard ATM cell format and that administrative header 42 can be any number of octets in length. As known to those having ordinary skill in the art, an octet comprises 8 bits of information. Although described with particular reference to the transportation of ATM cells

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over a DSL communication channel, the principles of the invention are applicable to all fixed length communication messages.

FIG. 3A is a schematic view illustrating the bit to symbol relationship of the communication message 31 of FIG. 2B. In accordance with an aspect of the invention, preamble 40 is placed at the beginning of every transmission (i.e., each communication message 31). Preamble 40 is followed by optional administrative header 42, which is then followed, if there is data to transmit, by one or more 53 octet ATM cell 44 and 45. Although illustrated using only two ATM cells, any number of ATM cells may follow preamble 40 and, if included, optional administrative header 42. The ATM cells are a stream of data information represented as a series of bits that are placed into each ATM cell.

The preamble 40 is also a series of bits, which are encoded into a number of communication symbols. Symbols are the representation of the bits to be transmitted, and are represented as signal points in a signal space constellation (to be described below with respect to FIGS. 4A and 4B). In accordance with one aspect of the invention, each of the bits in preamble 40 are encoded into symbols, an exemplar one of which is illustrated using reference numeral 55, at the lowest available bit rate that can be transmitted over the communication channel 16. For purposes of illustration only, the symbols that encode the bits in the preamble 40 shown in FIG. 3A are encoded at a rate of two (2) bits per symbol. However, any number of bits per symbol lower than that of the normally transmitted data rate can be used so long as the symbol rate allows a receiving device to more reliably decode those symbols. For example, if the normal data rate is five (5) bits per symbol, then a symbol rate of two (2) bits per symbol has a significantly (approximately 9 dB) higher noise margin than the five (5) bit per symbol data rate, thereby allowing the symbols that are encoded at the lower rate of two (2) bits per symbol to be very robustly and reliably decoded by a receiving device. In this manner, the preamble 40, which is sent at the beginning of every communication message 31, can be made sufficiently robust so that the chance that it will always be received error free is greatly increased. Although very robust, there are still situations in which the symbols into which the preamble bits are encoded can be corrupted. However, in accordance with another aspect of the invention, because the preamble 40 is sent at the beginning of every communication message 31, even if the preamble 40 is corrupted, only data following that preamble may be affected, i.e., lost due to corruption, if certain bits of the preamble are corrupted.

In accordance with another aspect of the invention, the first symbol 55 representing the first bits in the preamble 40 can be sent using an increased power level, thereby clearly and robustly delimiting the beginning of the communication message 31. The effect of this increased power level symbol 55 will be explained in greater detail below with respect to FIGS. 4A and 4B.

Still referring to FIG. 3A, if an administrative header 42 is present in communication message 31, then the bits that are contained in administrative header 42 will be encoded at a symbol rate of "N" bits per symbol, where N is the normal data rate. The normal data rate can be any data rate, for example, but not limited to, a value between 2 and 12 (inclusive) bits per symbol. For purposes of illustration, and for simplicity of explanation, the normal symbol rate can be five bits per symbol. This is represented by the group of symbols 56 into which all the bits of administrative header 42 and a portion of the bits of header 47 of ATM cell 44 are encoded.

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In accordance with another aspect of the invention, the first symbol used to encode bits from a particular cell that contains bits only from that cell will be encoded at a data rate lower than that of the standard data rate used for all other bits of each cell. For example, symbol 57 is the first symbol that contains bits only from ATM cell 44. The last symbol 65 of symbol group 56 contains bits from both administrative header 42 and ATM cell 44. Likewise, symbol 60 is the first symbol containing only bits from ATM cell 45. In accordance with this aspect of the invention, the symbols 57 and 60 will be encoded at a data rate that is two (2) bits per symbol lower than that of the preceding symbol (represented by N-2 where N is the number of bits per symbol used for encoding all other bits of the administrative header and ATM cells.) In this manner, because of the fixed length 53 octet ATM cells, by simple bit counting, the receiver will always know the first symbol encoding bits from a cell that contains only bits from this cell, and therefore has the special encoding described herein. These N-2 bits of the cell data are grouped for transmission and an additional bit (bit 54 for cell 44 or bit 61 for cell 45) is added for a total of N-1 bits encoded into symbol 57 or 60, respectively. This group of N-1 bits, represented by symbol 57 or 60, is encoded into a symbol and scaled for transmission with the scaling normally applied when encoding at N-1 bits per symbol. The extra bit 54 or 61 indicates whether or not the cell just started (ATM cell 44 or 45, respectively) is the last cell of the transmission. The extra bit 61 in symbol 60 is set to logic one to indicate that ATM cell 45 is the last cell of the transmission so that the receiver will know at the beginning of the receipt of ATM cell 45 that ATM cell 45 is the last cell in the transmission. For the same reason, bit 54 in symbol 57 set to zero so that the receiver will know that at least one more cell follows cell 44.

If N=2, then no bits are taken from the cell to encode the next symbol (since N-2=0). Since N-1=1, the next symbol contains just one bit, which is the last cell indicator. This effectively inserts an entire extra symbol in each cell. Nevertheless, the same encoding/decoding logic for this special symbol applies for any value of N $\geq$ 2.

Once the receiver knows that a particular cell is the last cell in the message, by simple counting it can readily identify the symbol that contains the last bits of the last cell. This is represented in FIG. 3A as symbol 51 or optionally symbol 53. Since the number of bits remaining to be transmitted in the last symbol (M) can be less than N, a modified encoding technique is preferable for this symbol. One option is to add one or more padding bits (P) 52 so that M+P=N. Another option is to encode the last group of bits at M bits per symbol as represented by symbol 53. This has the advantage of increased robustness for the transmission of these bits.

For simplicity, the following discussion does not address this second technique. Having recognized the last symbol of the transmission, the receiver does not attempt to demodulate and decode the signal on the line following this symbol since the transmitting station must now be sending silence.

It should be noted that although described as being encoded at N-1 bits per symbol, the symbols 57 and 60 containing the additional last cell indicator bit can be encoded at any symbol rate lower than that of the standard transmission rate (N bits per symbol). For example, if N is five (5), the specially encoded symbols could also be encoded at N-2 or three (3) bits per symbol so that they contain two (2) bits of cell data plus the last cell indicator bit. In this manner, the receiver can clearly and reliably decode the symbol 60, thereby providing a robust and reliable end of message delimiter.

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In accordance with this aspect of the invention, and to be described in further detail with respect to FIG. 3B, it is also desirable to have the ability to indicate that a message contains only an administrative header 42. In order to accomplish this, the first symbol containing data from the administrative header 42 can also be encoded using the higher noise margin N-1 bit per symbol encoding technique described above. For example, the first N-2 bits of the administrative header 42 can be combined with a last cell bit (such as bit 61 of symbol 60) and be encoded at the N-1 bit per symbol rate. This can provide the extra bit to indicate whether or not one or more ATM cells follow administrative header 42. An alternative technique is to simply include a bit in the preamble 40 that indicates whether an administrative header 40 follows the preamble. For simplicity, it has been assumed that this alternative technique is used with respect to FIG. 3A and in the following discussion.

Because each ATM cell is the smallest unit of a payload of ATM cells, and because all ATM cells have the same length, the first symbol of each cell that carries only bits of that cell can readily be identified. Because these bits are transmitted using the specially encoded symbol carrying two fewer bits than normal (as described above), the length of each cell is effectively increased by two bits. In some cases this can result in one extra symbol being needed to transmit the cell. In other cases an additional cell is not needed because the spare bits are available anyway (and would have ended up as the padding bits (P) 52 in FIG. 3A). Because the cells may be transmitted contiguously as a bit stream, the addition of one extra symbol may provide sufficient extra bits to cover the opening symbol of multiple following cells. For example, at eight (8) bits per symbol, in one (1) extra symbol is needed to cover the end of frame signaling overhead to transmit up to four (4) cells.

FIG. 3B is a schematic view illustrating, in further detail, the exemplary preamble 40 of FIG. 3A. The bit stream of preamble 40 comprises four (4) bits 62 that include information regarding the transmit rate (in bits per symbol) used to encode data following preamble 40 (the data comprising the optional administrative header and optional ATM cells), four (4) bits 63 that include information regarding the rate (also in bits per symbol) that the receiver is capable of receiving, two (2) bits 64 that identify the address of a remote DSL transceiver if the control DSL transceiver is transmitting (if a remote DSL transceiver is transmitting, then these two (2) bits 64 can represent the address of that remote DSL transceiver) and two (2) bits 66, which can be used to communicate the format of the message to follow. For example, the two (2) bits 66 can be used to advise a receiving device whether an administrative header 42 follows the preamble 40, whether both follow or whether only the preamble is being transmitted. The four (4) bits provided by symbols 55 and 67 and by symbols 68 and 69 can each encode as many as sixteen data encoding rates.

As mentioned above, the preamble 40 is sent at the beginning of each transmission. The twelve (12) bits that comprise the preamble 40 are encoded into symbols 55, 67, 68, 69, 70 and 71 in accordance with that described above. In accordance with an aspect of the invention, all of the symbols in preamble 40 are encoded at a low bit per symbol rate. In this example, all of the symbols are encoded at a rate of two (2) bits per symbol, however, any other low bit per symbol rate can be used with similar results. The low bit per symbol rate ensures a high signal-to-noise ratio for these symbols, thereby significantly decreasing the probability that these preamble symbols will be corrupted by noise on

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the communication channel. The payload data (administrative header and ATM cells) would typically be encoded at N bits per symbol only if transmission at this N bit per symbol rate has an acceptably low rate of errors (based on line length, signal strength, noise, distortion and other impairments that may be present). Otherwise, data transmission efficiency would suffer. Therefore, encoding the preamble at less than N bits per symbol allows a corresponding improvement in the reliability of transmitting this information such that it is highly unlikely to be corrupted. Since very few bits are needed to convey the information carried in the preamble, a very low rate can be used without seriously reducing the overall transmission efficiency.

In accordance with another aspect of the invention, the first symbol 55 is encoded at a rate of two (2) bits per symbol and has its energy increased to a point at which noise on the communication channel is unlikely to cause a receiver to erroneously interpret the first symbol 55 as silence. Likewise the increased energy makes it unlikely that noise on the communication channel will cause the receiver to erroneously interpret an interval of the silence that precedes each message as the starting symbol of a message. It has been found that an energy increase of 3dB is sufficient. This aspect of the invention will be described in greater detail below with respect to FIGS. 4A and 4B. In this manner, the beginning of each transmission can be clearly and robustly delimited. The remainder of the symbols 67, 68, 69, 70 and 71 that represent the bits in preamble 40 are all encoded at two (2) bits per symbol, but do not have their energy increased.

The four (4) transmit rate bits 62 inform a receiving DSL transceiver of the transmit rate of the information to follow the preamble 40. Sending this information in every message has significant benefits. It provides the transmitting transceiver the option of changing the encoding rate for the payload from one message to the next. Messages containing information that has been determined to be of high priority can be transmitted using a lower number of bits per symbol to improve the chances of its being received without errors. If the communications system intermittently has a reduced throughput demand, the transceivers may instantly reduce their data rates to improve robustness without adversely affecting real throughput. Finally, if a severe noise condition (such as an impulse caused by plain old telephone service (POTS) ringing signals on a subscriber line 16) happens to corrupt one or both of the symbols 55 and 67 that encode the transmit rate, only the payload data in this message will be improperly decoded. The receiver's memory of a corrupted rate value lasts only until the next transmission begins. This allows the transmit rate to potentially be changed for every message while at the same time avoiding the complexities of providing fail-safe communication of the rate, such as through use of an automatic repeat request (ARQ) protocol, that would be needed if the rate is set only when it is changed.

The receive rate bits 63 allow the transmitting device to communicate to the receiving device the maximum receive rate at which the transmitting device can receive. Inherently included in these receive rate bits 63 are commands that instruct the opposite device to either increase or decrease its transmit rate. This allows the responding transceiver to instantly modify the rate it uses for its next transmission to accommodate changes in the signal quality that have been detected at the opposite end of the line.

In accordance with an aspect of the invention, the address bits 64 need only be used when the control DSL transceiver

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100 is communicating with a plurality of remote DSL transceivers in what is commonly referred to as "multi-point" mode. When communicating in "multi-point" mode the address bits 64 include either the address of the remote DSL transceiver 150 that is to transmit next (if the transmission is sent by the control DSL transceiver 100) or the address of the responding remote DSL transceiver 150 (if the transmission is sent by the remote DSL transceiver 150). Sending these bits 64 at the lower bit rate of the preamble reduces the likelihood of a remote transceiver 150 not responding or of the incorrect remote transceiver 150 responding to a message from the control transceiver 100. Frequent occurrence of either of these two types of errors could adversely affect the overall data transmission efficiency of the line.

The format bits 66 indicate whether the optional administrative header 42 is being sent, whether one or more ATM cells are being sent, or whether both or neither are being sent. As described previously, the receiver uses this information in conjunction with the transmit rate from bits 62 to identify the special symbols at the start of each ATM cell and to determine the symbol that is the last in the message. Robust transmission of this information at the start of each message allows the transmitter to dynamically modify the message format as needed from one message to the next. Should one of the format bits be corrupted by an abnormally severe noise event, the "damage" is restricted to the current message only. To operate reliably, the receiver could have a "back up" method of recognizing the end of a message such as through detecting loss of signal energy for an extended duration.

FIG. 4A is a graphical illustration representing a two (2) bit per symbol signal space constellation and the increased energy symbol of FIG. 3B. The constellation points labeled "c" represent the points in a standard 2 bit per symbol constellation. For each constellation point "c" transmitted, the effect of noise can make the point appear to a receiver to have been moved with respect to where it was when it was transmitted. The dashed circle 76 surrounding constellation point 79 represents the space within which noise may move the point and still have the point reliably decoded by the receiver. The point 79 appears in a different place at the decoder due to noise induced in the communications channel 16. Each of the points "c" have a space about which they can move and still be reliably decoded by the receiver.

The circle 77 encloses the area surrounding the origin of the in-phase (horizontal) and quadrature (vertical) axes of FIG. 4A about which an interval of silence (no constellation point) can be moved by the same additive noise that can affect signal points. This additive noise could cause the silence to be interpreted by the decoder as one of the constellation points in a two (2) bit per symbol constellation due to the overlap of the decoding discrimination threshold circles 76 and 77. As shown, the circle 76 and the circle 77 have sufficient overlap in region 73 so that silence can easily be interpreted as one of the signal points "c". Conversely, one of the signal points "c" could also be interpreted by the decoder as silence.

For efficient operation, it is desirable that the beginning and end of each transmission be robustly and precisely identified (to within one (1) symbol interval). The beginning and end of each transmission are preceded and followed by silence on the line. Because the most efficient constellation encoding cannot allocate signal space to silence, it is impractical to reliably discriminate silence from signal when analyzing only a single symbol. In other words, it would be undesirable for silence that occurs before a message or after

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a message to be interpreted as a constellation point "c", and it would be undesirable for a constellation point "c" to be interpreted as silence. As mentioned above, this is possible due to the effect of noise altering the position of the constellation signal points "c" or the position of silence.

In accordance with an aspect of the invention, the first symbol (symbol 55 of FIG. 3B) in the preamble 40 is transmitted with increased energy, thereby increasing the probability that it will be reliably detected by the decoder of the receiving device. In this manner, the beginning of each transmission is clearly and robustly delimited. The signal point "b" in FIG. 4A is an exemplar one of four (4) two (2) bit per symbol constellation points that are transmitted at an increased energy level. While other increases may provide useful, a 3 dB increase is typically sufficient and does not increase the ratio of peak power to average power (PAR) of the transmitted signal. As illustrated, the signal point "b" is enclosed by dotted circle 78, within which the point "b" may move due to noise on the communication channel 16 and still be reliably decoded by the receiver. As shown, there is no overlap between circle 78 and circle 77. Accordingly, by boosting the energy of the first symbol (symbol 55 of FIG. 3B) transmitted in a communication message (31 of FIG. 3A), there is a significantly higher probability that the boosted symbol will be reliably decoded and not be mistaken for silence. Nor will silence be mistaken for this boosted energy first symbol. Preferably, the receiver places the threshold to discriminate signal from noise at one unit from the origin as shown by circle 77 in FIG. 4A.

FIG. 4B is a graphical illustration showing an exemplar grouping of constellation points representing different bit per symbol rates in accordance with an aspect of the invention. For example purposes only, assuming that normal data is encoded at five (5) bits per symbol, the black constellation points, an exemplar of one of which is illustrated using reference numeral 81, represent data encoded at five (5) bits per symbol. In accordance with an aspect of the invention, all the symbols in the preamble 40 are encoded at a rate of two (2) bits per symbol and are illustrated by the four (4) constellation points labeled "c" in FIG. 4B. These two (2) bit per symbol constellation points provide a higher signal-to-noise ratio (high margin) than do the normal data encoded at five (5) bits per symbol. This increased margin increases the probability that the receiver will reliably decode all the symbols in the preamble.

In accordance with another aspect of the invention, the four constellation points labeled "b" in FIG. 4B represent the first symbol (symbol 55 of FIGS. 3A and 3B), which energy is boosted by 3 dB. In this manner, the constellation points "b" representing the boosted symbol 55 of FIG. 3A and 3B will robustly and reliably communicate the beginning of a transmission. Circle 82 represents the maximum signal level of any symbol as the number of bits per symbol becomes arbitrarily large, but the average power of the transmitted signal is the same as it is for either the five (5) bits per symbol (81) or the two (2) bits per symbol (points "c") constellations shown. Therefore, as illustrated by circle 82, the instantaneous power required by the boosted symbol points "b" is not any higher than that used to send the normal data at any bits per symbol value. In this manner, the boosted symbol represented by constellation points "b" can be used to reliably indicate the start of a message without requiring a higher transmit level capability than that needed for normal data transmission. The non-boosted two (2) bit per symbol constellation points indicated as "c" (having a significantly higher signal-to-noise ratio than that of the normal five (5) bit per symbol data) are used to transmit all symbols of the preamble after the first symbol.

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FIG. 5 is a schematic view illustrating the communication message 31 of FIG. 3A and another aspect of the invention. Typically, it is desirable to scramble all the data bits in a communications message using a self-synchronizing scrambler so that all points in the signal constellation can be used. Unfortunately, the self-synchronizing capability of the scrambler carries the inherent disadvantage of error propagation and extension. A single bit in error in the received data stream is typically transformed by the self-synchronizing descrambling process into at least 3 erroneous bits that are separated by several bits that are not in error.

Typically, in switched-carrier operation, the scrambler setting (state) at the end of one transmission is preserved and used to begin scrambling the next message. (This enables full randomization of the encoding process so as to make full use of the available channel bandwidth.) Similarly, in a receiving device, when descrambling, the state of the descrambler that exists at the end of the previously received message is used to begin the descrambling process for the next received message. This means that the last state of the scrambler saved after scrambling the data portion of the message would then be used to begin scrambling the preamble bits of the next message.

Unfortunately, using this technique with the robust preamble 40 of the invention can lead to error propagation from the data portion of the communication message to the preamble 40. Allowing errors, which are more likely due to the larger number of bits per symbol, in the payload data to corrupt the data in the preamble due to the inherent error extension of the descrambling process significantly reduces the robustness of the preamble 40. In accordance with another aspect of the invention, a first scrambler can be used to scramble the information contained in the preamble 40 and a second scrambler can be used to scramble the data (i.e., the information in the ATM cells 44, 45, etc.)

As shown in FIG. 5, line 87 indicates that a first scrambler is used to scramble the preamble 40 of communication message 31 and also used to scramble the preamble of communication message 86. Similarly, line 88 indicates that a second scrambler is used to scramble the data portion of communication message 31 and the data portion of communication message 86. The message to message randomizing desirable for full usage of the available channel bandwidth can be maintained if the setting of the preamble scrambler (to be described with respect to FIG. 8) at the end of one preamble is used to begin the scrambling of the preamble of the next communication message 86. Because errors in the preamble are considered unlikely to occur, and because the bits received at the end of a previous preamble define the descrambler state used to descramble the next preamble, error extension from one message preamble into the preamble is also much less likely than in the single scrambler case.

An alternative to this that avoids the use of two scramblers is to save the state of the preamble scrambler after scrambling the preamble as the state to use to begin scrambling of the next preamble. This can be done instead of the conventional approach of using the state of the scrambler at the end of the message. This technique can also prevent errors at the end of one message from corrupting the preamble of the next transmission.

FIG. 6 is a schematic view illustrating the communication message 31 and the reduced line turn around delay made possible by an aspect of the invention. In time-domain duplex operation any periods during which no transceiver is transmitting represent loss of available bandwidth. To make

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most efficient usage of a communication line, it is desirable to minimize these periods. Some intervals of silence necessarily occur between transmissions because the transition from silence to the first symbol of the preamble is the manner in which the beginning of the next transmission is delimited. The process by which a transceiver makes the transition from receiving to transmitting is referred to as "line turn-around" and the time required may determine the minimum amount of silence that can occur between messages. Various aspects of the design and implementation of a time-domain duplex transceiver may result in increased delays in the line turn-around process. For example, transmitter filters and receiver equalizers have inherent delays. The analog-to-digital and digital-to-analog conversion process as well as the process of transferring digital samples between the signal processor and converters may have some inherent delays. If the signal processing is implemented in firmware there may be delays between the arrival of received signal samples and the time the processing can be performed. All of these factors may extend the line turn-around time to the point that transmission efficiency is significantly reduced.

As described above with respect to FIG. 3A, communication message 31 includes a specially encoded symbol 60 transmitted at a lower bit per symbol rate than that of the normal data encoding rate. The symbol encodes an additional bit 61 that indicates whether or not the ATM cell is the last cell in the communication message 31. If it is indicated to the receiver at the beginning of the last ATM cell 46 that the ATM cell 46 is the last cell in the communication message, (instead of waiting to the end of the ATM cell 46) line turn around delay can be reduced. As illustrated, if a receiving device must wait until the end of the last message in turn to learn that the message is complete, there will be a delay "d" between the time that the communication message 31 is received and the time at which the transmission of communication message 91a can begin. By having advance notification that the communication message is about to be complete, a remote DSL transceiver 150 can begin transmission of the next message before reception of the current message has been completed. By knowing the delay contributed by the factors such as those mentioned previously, the transceiver can begin the transmission process, indicated by communication message 91b, so as to reduce delay "d" as much as possible, potentially reducing it to the minimum value needed for the receiver to reliably detect the transition from silence to signal at the beginning of the next message.

FIG. 7 is a block diagram illustrating the control DSL transceiver 100 of FIG. 1. Although, described with respect to control DSL transceiver 100, the following description is equally applicable to a remote DSL transceiver 150. Control DSL transceiver 100 includes microprocessor 101, memory 102, transmitter 115 and receiver 120 in communication via logical interface 108. A bi-directional stream of ATM cells from a DTE is communicated via line 14 to the control DSL transceiver 100. Memory 102 includes end of transmission delimiting software 106 and robust preamble software 104. This software resides in memory 102 and executes in microprocessor 101 in order to achieve and perform the benefits of the present invention. Transmitter 115 communicates with line interface 109 via connection 112 in order to gain access to communication channel 16. Information received on communication channel 16 is processed by line interface 109 and sent via connection 111 to receiver 120.

Transmitter 115 includes, among other elements that are known to those having ordinary skill in the art, encoder 200 and modulator 117. Similarly, receiver 120 includes, among

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other elements that have been omitted for clarity, decoder 300 and demodulator 118.

FIG. 8 is a block diagram illustrating the encoder 200 of FIG. 7. The transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the first two (2) bits of the four (4) bits (62 of FIG. 3B) that define the current transmit rate from transmit rate element 206, via connection 212. This symbol is then forwarded to preamble scrambler 217, via connection 216 for scrambling, and is then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219. This encoded symbol is then forwarded via connection 226 to gain increase element 227 where its energy is increased by approximately 3 dB and is then sent via connection 228 to multiplexer 224 and over connection 254 to modulator 117.

The next two (2) bits of the transmit rate (62 of FIG. 3B) are then scrambled and encoded in the same way. Next, the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the four (4) bits representing the requested received rate from receive rate element 204, which bits are forwarded to multiplexer 214 via connection 211. These four (4) bits are then forwarded to preamble scrambler 217 where they are scrambled, and then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219 where they are encoded into a pair of symbols. These encoded symbols are forwarded directly via connection 226 to multiplexer 224 and then forwarded via connection 254 to modulator 117.

If there are multiple remote DSL transceivers 150 and 153, then the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the two (2) bits representing the remote address from remote address element 202, which bits are then forwarded via connection 209 to multiplexer 214. These two (2) bits are then forwarded via connection 216 to preamble scrambler 217, which scrambles the bits and forwards them via connection 218 to the two (2) bit per symbol preamble encoder 219. The two (2) bit per symbol preamble encoder 219 encodes the bits and transfers the encoded symbol via connection 226 through multiplexer 224 and then via connection 254 to modulator 117.

Transmit sequencer 236 senses if an administrative header 42 and/or ATM cells 44, 45, 46 are available for transmission via connections 232 and 234, respectively, and uses this information to prepare the message format indicator which is loaded by the transmit sequencer 236 via connection 207. The transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the two (2) bits representing the message format from element 201, which bits are then forwarded via connection 208 to multiplexer 214. These two (2) bits are then forwarded via connection 216 to preamble scrambler 217, which scrambles the bits and forwards them via connection 218 to the two (2) bit per symbol preamble encoder 219. The two (2) bit per symbol preamble encoder 219 encodes the bits and transfers the encoded symbol via connection 226 through multiplexer 224 and then via connection 254 to modulator 117.

Next, transmission of either the administrative header 42 or the ATM cell payload begins by transmit sequencer 236 sending a command via connection 235 to multiplexer 241 to select either the administrative header 42 via element 229 or payload data via element 231. These bits are supplied through multiplexer 241 via connections 239 and 238 and are then forwarded via connection 244 to payload scrambler 246. Payload scrambler 246 scrambles the bits and forwards them via connection 248 to N bit per symbol data encoder 249 and N-1 bit per symbol data encoder 251. As mentioned

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above with respect to FIG. 5, payload scrambler 246 may use as its initial state either the state that exists at the end of scrambling the preamble (supplied via connection 247) or the state that exists after completion of scrambling the payload portion of the previous message. As mentioned above with respect to FIG. 3A, all the data bits are encoded at an N bit per symbol data rate by data encoder 249 and forwarded via connection 257 to multiplexer 224 until the first symbol containing only bits from a new ATM cell is detected. This symbol is encoded at a rate of N-1 bits per symbol by N-1 bit per symbol data encoder 251 and forwarded via connection 256 to multiplexer 224. The index for this symbol as delivered to payload scrambler 246 is formed by selecting the first N-2 bits of the first octet of the cell and adding an additional bit (i.e., bit 54 or bit 61 of FIG. 3A) representing the state of the last cell signal 237 as selected via multiplexer 241. When instructed by transmit sequencer 236 via connection 252, the multiplexer 224 selects the symbols from either N bit per symbol data encoder 249 or from N-1 bit per symbol data encoder 251 and forwards these symbols via connection 254 to modulator 117.

Transmit sequencer 236 uses the payload bits per symbol value N received via connection 212 to determine the number of symbols to encode for each cell and to determine which symbol is to be encoded at the N-1 bits per symbol rate and contain the last cell indicator bit. After completing transmission of the message, transmit sequencer 236 commands multiplexer 224 via connection 252 to select silence 221 via connection 222 as the input to the modulator 117.

FIG. 9 is a block diagram illustrating the decoder 300 of FIG. 7. A received transmission stream is received in demodulator 118, where it is demodulated in accordance with techniques known to those having ordinary skill in the art. The first symbol is forwarded via connection 301 to gain reduction element 302. Gain reduction element 302 reduces the gain of the first symbol and supplies that reduced energy symbol via connection 304 to multiplexer 306. Receive sequencer 328 sends a signal to multiplexer 306 via connection 354 instructing multiplexer 306 to select that reduced gain symbol and transfer it via connection 307 to two (2) bit per symbol preamble decoder 308. The decoded bits from the first symbol are then sent via connection 309 to preamble descrambler 311. Preamble descrambler 311 descrambles the first bits in the transmission and forwards them via connection 312 to the multiplexer 314. When instructed by receive sequencer 328 via connection 332, the multiplexer 314 forwards these bits via connection 324 to transmit rate element 236.

The following preamble symbols are all forwarded via connection 301 directly to multiplexer 306, which forwards these symbols via connection 307 for decoding by two (2) bit per symbol preamble decoder 308. The decoded bits are forwarded via connection 309 to preamble descrambler 311 as mentioned above. These bits are then forwarded in order via connections 324, 321, 318 and 316 to transmit rate element 326, receive rate element 322, remote address element 319 and message format element 317, respectively.

Next, the administrative header symbols and ATM cell data symbols that have been encoded at N bits per symbol are forwarded via connection 301 to N bit per symbol data decoder 337 and the ATM cell data symbols that have been encoded at N-1 bits per symbol are forwarded via connection 301 to N-1 bit per symbol data decoder 339. These symbols are decoded and the decoded bits are transferred via connections 338 and 341 to multiplexer 342. Similarly, as mentioned above with respect to FIG. 8, receive sequencer

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328 insures that the symbols encoded at the rate of  $N-1$  bits per symbol are forwarded via connection 301 to  $N-1$  bit per symbol data decoder 339, which forwards the decoded bits via connection 341 to multiplexer 342. As shown, the value of  $N$ , which is the bits per symbol value used for the  $N$  bits per symbol, or  $N-1$  bits per symbol decoding is controlled by the just received transmit rate bits that have been stored in transmit rate element 326.

At the appropriate time, receive sequencer 328 commands the multiplexer 342 via connection 347 to forward the bits via connection 344 to payload descrambler 336. In accordance with an aspect of the invention, the preamble descrambler 311 operates only on the preamble bits and the payload descrambler 336 operates only on the payload bits. As mentioned above with respect to FIG. 5, the payload descrambler may use as its initial state either the state of the preamble descrambler at the end of descrambling the preamble as supplied via connection 334 or the state of the payload descrambler at the end of descrambling the payload bits of the previous message. The descrambled payload bits are then forwarded via connection 346 to multiplexer 349. When ordered by receive sequencer 328 via connection 331, the multiplexer 349 forwards the administrative header bits via connection 351 and the payload data bits via connection 352. These bits are then forwarded via logical interface 108 to microprocessor 101 for processing (FIG. 7). Receive sequencer 328 determines the presence or absence of the administrative header and ATM cells via the just received message format bits that have been stored in element 317 and provided to receive sequencer 328 via connection 327. When the bits for each symbol containing the last message bit are available at multiplexer 349, receive sequencer 328 directs the  $N-2$  bits of payload data to the payload data element 356 via connection 352 and receives the last cell bit via connection 329. Receive sequencer 328 uses the current bits per symbol value for payload data received via connection 324 to determine the beginning and end of each cell. Based on the message format and the value of the last cell indicator bit, receive sequencer 328 determines when the last symbol of the message has been decoded and instructs demodulator 118 (FIG. 7) to stop delivering demodulated symbols.

In an alternative embodiment, the special encoding of the last cell as described above in FIG. 3A can be omitted and an "eye pattern closure test" can be used to detect the end of the message. In such a situation where it is acceptable to lose the advanced notification of the end of the transmission, beneficial alternative uses for the special encoding of the first bits of each cell are possible. For example, this special encoding as described above with respect to FIG. 3A wherein  $N-2$  bits are encoded for the first full bytes of each cell, can be used to indicate whether or not the ATM cell header (e.g., ATM header 47 of FIG. 2B) is present. This can be useful in the situation in which a string of ATM cells have exactly the same header. This can happen, for example, for ATM adaptation layer 5 (AAL5) cells that carry data from a single protocol data unit (PDU) if no other cells have been interleaved. The single extra bit (bit 61 of FIG. 3A) provided by the encoding described above with respect to FIG. 3A, can be used to indicate whether or not the following cell contains a header. If the bit 61 indicates that there is no header, the receiver copies the last header received ahead of the payload octets of this next cell before forwarding it to the ATM layer. Advantageously, this reduces the approximate 10 percent overhead imposed by the five (5) octet header (47 of FIG. 2B).

It should be emphasized that the above-described embodiments of the present invention, particularly any "preferred"

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embodiments, are merely possible examples of implementations, merely set forth for a clear understanding of the principles of the invention. Many variations and modifications may be made to the above-described embodiment(s) of the invention without departing substantially from the spirit and principles of the invention. For example, the robust preamble and transmission delimiting system and method are applicable to all switched-carrier transmission methodologies in which it is desirable to reliably convey channel establishment information and reliably delimit the beginning and end of each communication message. All such modifications and variations are intended to be included herein within the scope of the present invention.

Therefore, having thus described the invention, at least the following is claimed:

1. A system for robust transmission delimiting, comprising:

a communication message including a preamble, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

an encoder configured to encode the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel.

2. A system for robust transmission delimiting, comprising:

a communication message including a preamble, the preamble including a plurality of bits representing communication link control information; and

an encoder configured to encode the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel,

wherein the preamble includes information that defines a rate at which data following the preamble has been encoded for transmission.

3. The system as defined in claim 2, further comprising a gain boost element configured to increase the energy of the first symbol index to reliably indicate the beginning of the communication message.

4. The system as defined in claim 2, wherein the preamble includes information defining a maximum rate at which a first transceiver that is sending the preamble is able to receive transmissions from a second transceiver that is receiving the preamble.

5. The system as defined in claim 2, wherein the preamble indicates whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

6. The system as defined in claim 2, wherein the preamble indicates whether administrative information follows the preamble.

7. The system as defined in claim 5, further comprising: a first scrambler configured to scramble the preamble; and a second scrambler configured to scramble the data, wherein a state of the scrambler used to scramble the bits that comprise the preamble is the state that existed when scrambling of a previous preamble was completed.

8. The system as defined in claim 5, wherein the data portion of the communication message comprises fixed size units, the fixed size units comprising a plurality of bits and

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wherein the bits are encoded into symbol indices such that, for each of the fixed size units, one symbol index is encoded differently from the other symbols.

9. The system as defined in claim 8, wherein the differently encoded symbol index further comprises an extra bit that indicates whether the fixed size unit from which the other bits of the differently encoded symbol indices are obtained is the last one transmitted in a message.

10. The system as defined in claim 8, wherein the differently encoded symbol index is encoded at a data rate lower than that of the other symbols carrying message data.

11. A system for delimiting the end of a transmission, comprising:

a communication message segmented into a plurality of fixed size units, each fixed size unit including a plurality of bits; and

an encoder configured to encode the plurality of bits into a plurality of symbol indices at a first data rate, the encoder also configured to encode at a second rate when producing the first symbol index in the plurality of symbol indices that contains only bits from each fixed size unit, where the second rate is lower than the first rate.

12. A method for robust transmission delimiting, the method comprising the steps of:

applying a preamble to a communication message, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

13. A method for robust transmission delimiting, the method comprising the steps of:

applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information;

encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel; and

including information in the preamble defining a rate at which data following the preamble has been encoded for transmission.

14. The method as defined in claim 13, further comprising the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

15. The method as defined in claim 13, further comprising the step of including information in the preamble defining a maximum rate at which a transceiver that is sending the preamble is able to receive transmissions from a transceiver that is receiving the preamble.

16. The method as defined in claim 13, further comprising the step of using the preamble to indicate whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

17. The method as defined in claim 13, further comprising the step of using the preamble to indicate whether administrative information follows the preamble.

18. The method as defined in claim 16, further comprising the steps of:

scrambling the preamble using a first scrambler; and scrambling the data using a second scrambler; and

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scrambling the bits in the preamble using the state of the scrambler that existed when scrambling of the previous preamble was complete.

19. The method as defined in claim 16, wherein the data portion of the communication message comprises fixed size units, the fixed size units comprising a plurality of bits, and wherein the bits that comprise each of the fixed size units are encoded into symbol indices such that for each of the fixed size units, one symbol index is encoded differently from the other symbols.

20. The method as defined in claim 19, further comprising the step of including in said differently encoded symbol index an extra bit that indicates whether the fixed size unit from which the other bits of said differently encoded symbol indices are obtained is the last one transmitted in a message.

21. The method as defined in claim 19, further comprising the step of encoding the differently encoded symbol index at a data rate lower than that of the other symbols carrying message data.

22. A method for delimiting the end of a transmission, the method comprising the steps of:

segmenting a communication message into a plurality of units, each unit including a plurality of bits and having a fixed size;

encoding a plurality of the bits in the plurality of units into a plurality of symbol indices, the symbol indices being encoded at a first rate; and

encoding one symbol index of the plurality of symbol indices at a rate lower than the first rate, the one symbol index containing bits from only one of the plurality of units.

23. A system for robust transmission delimiting, comprising:

means for applying a preamble to a communication message, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

means for encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

24. The system as defined in claim 23, further comprising means for increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

25. A system for robust transmission delimiting, comprising:

means for applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information;

means for encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel; and

means for including information in the preamble defining a rate at which data following the preamble has been encoded for transmission.

26. The system as defined in claim 25, further comprising means for including information in the preamble defining a maximum rate at which a transceiver that is sending the preamble is able to receive transmissions from a transceiver that is receiving the preamble.

27. The system as defined in claim 25, further comprising means for using the preamble to indicate whether a data

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portion follows the preamble and, if so, the format and type of data that follows the preamble.

28. The system as defined in claim 25, further comprising means for using the preamble to indicate whether administrative information follows the preamble.

29. The system as defined in claim 27, further comprising: means for scrambling the preamble using a first scrambler;

means for scrambling the data using a second scrambler; and

means for scrambling the bits in the preamble using the state of the scrambler that existed when scrambling of the previous preamble was complete.

30. The system as defined in claim 27, wherein the data portion of the communication message comprises fixed size units, the fixed size units comprising a plurality of bits; and

means for encoding the bits that comprise each of the fixed size units into symbol indices such that for each of the fixed size units, one symbol index is encoded differently from the other symbols.

31. The system as defined in claim 30, further comprising means for including in said differently encoded symbol index an extra bit that indicates whether the fixed size unit from which the other bits of said differently encoded symbol indices are obtained is the last one transmitted in a message.

32. The system as defined in claim 30, further comprising means for encoding the differently encoded symbol index at a data rate lower than that of the other symbols carrying message data.

33. A system for delimiting the end of a transmission, comprising:

means for segmenting a communication message into a plurality of fixed size units, each unit including a plurality of bits;

means for encoding a plurality of the bits in the units into a plurality of symbol indices, the symbol indices being encoded at a first rate; and

means for encoding at a second rate when producing the first symbol index in the plurality of symbol indices that contains only bits from each fixed size unit, where the second rate is lower than the first rate.

34. A computer readable medium having a program for robust transmission delimiting, the program comprising logic for performing the steps of:

applying a preamble to a communication message, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

35. The program as defined in claim 34, further comprising logic for performing the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

36. A computer readable medium having a program for robust transmission delimiting, the program comprising logic for performing the steps of:

applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information;

encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per

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symbol rate relative to the maximum rate capable of being transmitted over a communication channel; and including information in the preamble defining a rate at which data following the preamble has been encoded for transmission.

37. The program as defined in claim 36, further comprising logic for performing the step of including information in the preamble defining a maximum rate at which a transceiver that is sending the preamble is able to receive transmissions from a transceiver that is receiving the preamble.

38. The program as defined in claim 36, further comprising logic for performing the step of using the preamble to indicate whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

39. The program as defined in claim 36, further comprising logic for performing the step of using the preamble to indicate whether administrative information follows the preamble.

40. The program as defined in claim 38, further comprising logic for performing the steps of:

scrambling the preamble using a first scrambler;

scrambling the data using a second scrambler; and

scrambling the bits in the preamble using the state of the scrambler that existed when scrambling of the previous preamble was complete.

41. The program as defined in claim 38, wherein the data portion of the communication message comprises fixed size units, the fixed size units comprising a plurality of bits; and

wherein the bits that comprise each of the fixed size units are encoded into symbol indices such that for each of the fixed size units, one symbol index is encoded differently from the other symbols.

42. The program as defined in claim 41, further comprising logic for performing the step of including in said differently encoded symbol index an extra bit that indicates whether the fixed size unit from which the other bits of said differently encoded symbol indices are obtained is the last one transmitted in a message.

43. The program as defined in claim 41, further comprising logic for performing the step of encoding the differently encoded symbol index at a data rate lower than that of the other symbols carrying message data.

44. A computer readable medium having a program for delimiting the end of a transmission, the program comprising logic to perform the steps of:

segmenting a communication message into a plurality of fixed size units, each unit including a plurality of bits;

encoding a plurality of the bits in the fixed sized units into a plurality of symbol indices, the symbol indices being encoded at a first rate; and

encoding at a second rate when producing the first symbol index in the plurality of symbol indices that contains only bits from each fixed size unit, where the second rate is lower than the first rate.

45. A method for delimiting the end of a transmission, the method comprising the steps of:

segmenting a communication message into a plurality of fixed size units, each unit including a plurality of bits; encoding the first N bits in a unit into a first symbol index, the first symbol index being encoded at a first rate, N being less than the fixed size; and

encoding the remaining bits in the plurality of units into a plurality of symbol indices at a rate greater than the first rate.

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46. The system as defined in claim 11, further comprising a gain boost element configured to increase the energy of the first symbol index to reliably indicate the beginning of the communication message.

47. The system as defined in claim 11, wherein the preamble indicates whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

48. The method as defined in claim 22, further comprising the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

49. The method as defined in claim 22, further comprising the step of using the preamble to indicate whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

50. The system as defined in claim 33, further comprising means for increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

51. The system as defined in claim 33, further comprising means for using the preamble to indicate whether a data

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portion follows the preamble and, if so, the format and type of data that follows the preamble.

52. The program as defined in claim 44, further comprising logic for performing the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

53. The program as defined in claim 44, further comprising logic for performing the step of using the preamble to indicate whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

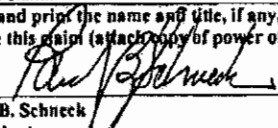
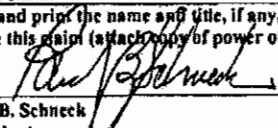
54. The method as defined in claim 45, further comprising the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

55. The method as defined in claim 45, further comprising the step of using the preamble to indicate whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

\* \* \* \* \*

**Exhibit B**

S&amp;S COPY

<b>UNITED STATES BANKRUPTCY COURT SOUTHERN DISTRICT OF NEW YORK</b> <b>P.O. BOX 5059</b> <b>BOWLING GREEN STATION</b> <b>NEW YORK, NY 10274</b>		<b>ADMINISTRATIVE EXPENSE CLAIM</b>	
<b>Name of Debtor Against Which Claim is Held</b> <b>Adelphia Communications Corp. and other</b> <b>Debtors listed on Exhibit A attached hereto</b>		<b>Chapter 11</b> <b>Case No. 02-41729 (REG)</b> <b>Jointly Administered</b>	
<small>NOTE: This form should be used to make a claim for an administrative expense arising after the commencement of the case. A request for payment of an administrative expense may be filed pursuant to 11 U.S.C. § 503.</small>			
<b>Name and address of Creditor:</b> <b>Rembrandt Technologies, LP</b> <b>401 City Avenue, Suite 815</b> <b>Bala Cynwyd, PA 19004</b>		<input type="checkbox"/> Check box if you are aware that anyone else has filed a proof of claim relating to your claim. Attach copy of statement giving particulars. <input type="checkbox"/> Check box if you have never received any notices from the bankruptcy court in this case. <input type="checkbox"/> Check box if the address differs from the address on the envelope sent to you by the court.	
<b>Notices should be sent to:</b> <b>Susman Godfrey L.L.P.</b> <b>590 Madison Avenue</b> <b>New York, NY 10022</b> <b>Attn: Tibor L. Nagy, Esq.</b>			
<b>Creditor's Telephone Number</b> <b>(610) 667-9685</b>		<b>Check Here</b> <input type="checkbox"/> replaces <input type="checkbox"/> supplements <input type="checkbox"/> amends a previously filed claim, dated: _____	
<b>ACCOUNT OR OTHER NUMBER BY WHICH CREDITOR IDENTIFIES DEBTOR</b>			
<b>1. Basis for Claim</b> <input type="checkbox"/> Goods sold/Services Performed <input type="checkbox"/> Contract/Lease (other than trading contracts) <input type="checkbox"/> Trading contract <input type="checkbox"/> Money loaned <input type="checkbox"/> Litigation		<input type="checkbox"/> Guarantees <input type="checkbox"/> Taxes <input checked="" type="checkbox"/> Other <u>See Exhibit A attached hereto</u> (explain) If your claim is for retiree benefits, wages, salary, or compensation, you should complete the Employee Proof of Claim Form rather than this form.	
<b>2. Date debt was incurred: See Exhibit A, attached hereto</b>		<b>3. If court judgment, date obtained:</b>	
<b>4. Pursuant to 11 U.S.C. § 503(a), "an entity may timely file a request for payment of an administrative expense, or may tardily file such request if permitted by the court for cause." 11 U.S.C. § 503(b) describes those administrative expenses which may be allowed in a debtor's chapter 11 case.</b>			
<b>5. TOTAL AMOUNT OF ADMINISTRATIVE CLAIM</b> <b>\$ SEE EXHIBIT A ATTACHED HERETO</b>			
<b>6. Supporting Documents: Attach copies of supporting documents, such as promissory notes, purchase orders, invoices, itemized statements of running accounts, contracts, court judgments, mortgages, security agreements, and evidence of perfection of lien. DO NOT SENT ORIGINAL DOCUMENTS. If the documents are not available, explain. If the documents are voluminous, attach a summary.</b> <b>7. Date-Stamped Copy: To receive an acknowledgment of the filing of your claim, enclose a stamped, self-addressed envelope and copy of this proof of claim.</b>		<b>THIS SPACE IS FOR COURT USE ONLY</b> <div style="text-align: center;">   <b>Paul B. Schneek</b>  <b>President</b> </div>	
<b>Date:</b> <b>September 13, 2006</b>		<b>Sign and print the name and title, if any, of the creditor or other person authorized to file this claim (attach copy of power of attorney, if any):</b> <div style="text-align: center;">   <b>Paul B. Schneek</b>  <b>President</b> </div>	
<b>Penalty for presenting fraudulent claim: Fine of up to \$500,000 or imprisonment for up to 5 years, or both. 18 U.S.C. §§ 157 and 355</b>			

U.S. BANKRUPTCY COURT  
 FILED  
 2006 SEP 13 P 3:58  
 S.D.N.Y.

**EXHIBIT A**

**Exhibit A**

**ADMINISTRATIVE EXPENSE PROOF OF CLAIM  
OF REMBRANDT TECHNOLOGIES, LP  
AGAINST ADELPHIA COMMUNICATIONS CORPORATION, ET AL.**

**Item 1. Basis for Claim**

Rembrandt Technologies, LP ("Rembrandt" or the "Claimant"), asserts the administrative expense claims (collectively, the "Administrative Expense Claim" or the "Claim") against Adelphia Communications Corporation ("ACC"), Century-TCI California, L.P., Century-TCI California Communications, L.P., Century-TCI Distribution Company, LLC, Century-TCI Holdings, LLC, Parnassos Communications, L.P., Parnassos Distribution Company I, LLC, Parnassos Distribution Company II, LLC, Parnassos, L.P., Parnassos Holdings, LLC, and Western NY Cablevision, L.P. (collectively, and other than ACC, the "JV Debtors") in chapter 11 cases pending in the Southern District of New York and jointly administered under case number 02-41729 (REG) (ACC and the JV Debtors are collectively, the "Debtors")<sup>1</sup> set forth in the complaint in the adversary proceeding captioned *Rembrandt Technologies, LP v. Adelphia Communications Corporation*, attached hereto as Exhibit B (the "Complaint").

**Item 2. Date Debt Was Incurred**

The Administrative Expense Claim arose during the period beginning on June 25, 2002 (the "June Petition Date") with respect to certain of the Debtors and on October 5, 2005 (together with the June Petition Date, the "Petition Date") with respect to certain other Debtors, and in each case ending upon the sale of substantially all of the Debtors' business assets on July 31, 2006 (such period, the "Post-Petition Period").

**Items 4 & 5. Request for Payment of Administrative Expense Claim**

Claimant hereby requests the payment of an amount not less than \$130.3 million in respect of, but not limited to, the following, in each case as set forth in the Complaint:

**(a) Infringement of Patent No. 5,710,761**

Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 5,710,761, entitled "Error Control Negotiation Based on Modulation" ("the '761 patent."). The '761 patent was duly and legally issued by the United States Patent and Trademark Office on January 20, 1998, after full and fair examination.

During the Post-Petition Period, the Debtors have infringed the '761 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '761 patent, in this district and otherwise within the

<sup>1</sup> Claimant submits this one, consolidated administrative proof of claim against the Debtors as the Debtors have not, upon information and belief, publicly disclosed the information necessary to allocate the Claim against each Debtor.

United States. For example, the Debtors infringed the '761 patent by providing high-speed cable modem internet products and services to subscribers.

**(b) Infringement of Patent No. 5,778,234**

Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 5,778,234, entitled "Method for Downloading Programs" ("the '234 patent."). The '234 patent was duly and legally issued by the United States Patent and Trademark Office on July 7, 1998, after full and fair examination.

During the Post-Petition Period, the Debtors have infringed the '234 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '234 patent, in this district and otherwise within the United States. For example, the Debtors infringed the '234 patent by providing high-speed cable modem internet products and services to subscribers.

**(c) Infringement of Patent No. 6,131,159**

Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 6,131,159, entitled "System for Downloading Programs" ("the '159 patent."). The '159 patent was duly and legally issued by the United States Patent and Trademark Office on October 10, 2000, after full and fair examination.

During the Post-Petition Period, the Debtors have infringed the '159 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '159 patent, in this district and otherwise within the United States. For example, the Debtors infringed the '159 patent by providing high-speed cable modem internet products and services to subscribers.

**(d) Infringement of Patent No. 6,950,444**

Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 6,950,444, entitled "System and Method for a Robust Preamble and Transmission Delimiting in a Switched-Carrier Transceiver" ("the '444 patent."). The '444 patent was duly and legally issued by the United States Patent and Trademark Office on September 27, 2005, after full and fair examination.

During the Post-Petition Period, the Debtors have infringed the '444 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '444 patent, in this district and otherwise within the United States. For example, the Debtors infringed the '444 patent by providing high-speed cable modem internet products and services to subscribers.

As set forth in the Complaint and upon information and belief, the Debtors' infringement of the patents described above was willful, entitling Rembrandt to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

As the Debtors have not, upon information and belief, publicly disclosed the information necessary to allocate the Claim against each ACC subsidiary and affiliate that is a chapter 11 debtor, the Claimant reserves the right to amend this Administrative Proof of Claim to, among other things, assert the Claim against such entities.

**Item 6. Supporting Documentation**

The Complaint is attached hereto as Exhibit B and copies of any other relevant materials will be provided upon request.

**Claimant reserves the right to amend and/or supplement this Administrative Expense Proof of Claim at any time and in any manner, and to file additional proofs of claim for additional claims. In addition, the Claimant reserves the right to attach or bring forth additional documents supporting its Claim and additional documents that may become available after further investigation and discovery.**

**Claimant is continuing to investigate the elements of the Claim, and this Administrative Expense Proof of Claim is being filed under the compulsion of the Administrative Expense Bar Date of September 14, 2006 with respect to the JV Debtors. The filing of this Administrative Expense Proof of Claim shall not constitute: (a) a waiver or release of the rights of Claimant against any of the Debtors or any other person or property; or (b) a waiver of the Claimant to contest the jurisdiction of this Court with respect to the subject matter of the Claim, any objection or other proceeding commenced with respect thereto or any other proceeding commenced in this case against or otherwise involving the Claimant.**

**EXHIBIT B**



2. Defendant Adelphia Communications Corporation ("ACC") is a corporation organized under the laws of the State of Delaware. On June 25, 2002, ACC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York in a case captioned *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG). That case remains pending in the bankruptcy court. ACC's principal place of business on the Petition Date was located in Coudersport, Pennsylvania, and is currently located in Greenwood Village, Colorado. ACC was one of the leading cable and telecommunications companies in the United States. Since seeking bankruptcy protection on June 25, 2002, ACC continued to provide cable internet and television services to consumers throughout the United States until the sale of substantially all of its assets on July 31, 2006.

3. Defendant Century-TCI California, LP is a partnership organized under the laws of the State of Delaware. Century-TCI California, LP is an affiliate of ACC. On June 25, 2002, Century-TCI California, LP filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Century-TCI California, LP's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

4. Defendant Century-TCI California Communications, LP is a partnership organized under the laws of the State of Delaware. Century-TCI California Communications, LP is an affiliate of ACC. On June 25, 2002, Century-TCI California Communications, LP filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Century-TCI California Communications, LP's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

5. Defendant Century-TCI Distribution Company, LLC is a limited liability company organized under the laws of the State of Delaware. Century-TCI Distribution Company, LLC is an affiliate of ACC. On October 6, 2005, Century-TCI Distribution Company, LLC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Century-TCI Distribution Company, LLC's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

6. Defendant Century-TCI Holdings, LLC is a corporation organized under the laws of the State of Delaware. Century-TCI Holdings, LLC is an affiliate of ACC. On June 25, 2002, Century-TCI Holdings, LLC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Century-TCI Holdings, LLC's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

7. Defendant Parnassos Communications, LP is a partnership organized under the laws of the State of Delaware. Parnassos Communications, LP is an affiliate of ACC. On June 25, 2002, Parnassos Communications, LP filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Parnassos Communications, LP's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

8. Defendant Parnassos Distribution Company I, LLC is a limited liability company organized under the laws of the State of Delaware. Parnassos Distribution Company I, LLC is an affiliate of ACC. On October 6, 2005, Parnassos Distribution Company I, LLC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of

New York. Parnassos Distribution Company I, LLC's bankruptcy proceedings are jointly administered with *In re Adelfhia Communications Corporation*, Case No. 02-41729 (REG).

9. Defendant Parnassos Distribution Company II, LLC is a limited liability company organized under the laws of the State of Delaware. Parnassos Distribution Company II, LLC is an affiliate of ACC. On October 6, 2005, Parnassos Distribution Company II, LLC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Parnassos Distribution Company II, LLC's bankruptcy proceedings are jointly administered with *In re Adelfhia Communications Corporation*, Case No. 02-41729 (REG).

10. Defendant Parnassos Holdings, LLC is a corporation organized under the laws of the State of Delaware. Parnassos Holdings, LLC is an affiliate of ACC. On June 25, 2002, Parnassos Holdings, LLC filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Parnassos Holdings, LLC's bankruptcy proceedings are jointly administered with *In re Adelfhia Communications Corporation*, Case No. 02-41729 (REG).

11. Defendant Parnassos, LP is a partnership organized under the laws of the State of Delaware. Parnassos, LP is an affiliate of ACC. On June 25, 2002, Parnassos, LP filed a petition in bankruptcy under Chapter 11 in the United States Bankruptcy Court for the Southern District of New York. Parnassos, LP's bankruptcy proceedings are jointly administered with *In re Adelfhia Communications Corporation*, Case No. 02-41729 (REG).

12. Defendant Western NY Cablevision, LP is a partnership organized under the laws of the State of Delaware. Western NY Cablevision, LP is an affiliate of ACC. On June 25, 2002, Western NY Cablevision, LP filed a petition in bankruptcy under Chapter 11 in the United

States Bankruptcy Court for the Southern District of New York. Western NY Cablevision, LP's bankruptcy proceedings are jointly administered with *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG).

13. On information and belief, Defendants are liable for the infringement of Rembrandt's patents as alleged herein. Rembrandt makes these allegations with regard to particular Defendants based on a review of publicly available information. Other affiliates of ACC may also be liable for infringement of these patents. Rembrandt intends to amend this pleading to add other ACC affiliates who have infringed Rembrandt's patents or, if appropriate, to dismiss Defendants who are shown not to have engaged in any infringing activity.

#### **JURISDICTION AND VENUE**

14. This is an action for patent infringement arising under the law of the United States relating to patents, including, *inter alia*, 35 U.S.C. §§ 271, 281, 284 and 285. This court has jurisdiction over such federal question claims pursuant to 28 U.S.C. §§ 1331 and 1338(a).

15. For the avoidance of doubt and for the sake of clarity, Plaintiffs hereby explicitly state that all acts of infringement alleged herein relate solely to actions taken by Defendants *after* their filing for bankruptcy in this district on June 25, 2002 or October 6, 2005, as applicable, and *before* the acquisition by Time Warner Cable and Comcast on July 31, 2006 (such period for each Defendant, the "Post-Petition Period"). Plaintiffs hereby explicitly state and affirm that they are not seeking relief for any actions of Defendants that occurred prior to the filing of ACC's bankruptcy petition. ACC continued to operate its cable internet and television businesses after June 25, 2002 and prior to its acquisition. In doing so, as alleged in greater detail below, ACC engaged in post-petition acts of infringement that have damaged Rembrandt.

It is solely based on these post-petition actions, and for relief under the United States patent laws, that Rembrandt brings this action.

16. This Court has personal jurisdiction over the Defendants because one or more events giving rise to the causes of action herein occurred in this district and because the Defendants have submitted to the jurisdiction of this Court.

17. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b) and 1409(a).

**COUNT I: INFRINGEMENT OF U.S. PATENT NO. 5,710,761**

18. Rembrandt refers to and incorporates herein the allegations of Paragraphs 1-17 above.

19. Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 5,710,761, entitled "Error Control Negotiation Based on Modulation" ("the '761 patent."). A true copy of the '761 patent is attached as Exhibit A.

20. The '761 patent was duly and legally issued by the United States Patent and Trademark Office on January 20, 1998, after full and fair examination.

21. During the Post-Petition Period, the Defendants have directly or indirectly infringed the '761 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '761 patent, in this district and otherwise within the United States. For example, Defendants infringed the '761 patent by providing high-speed cable modem internet products and services to subscribers.

22. Rembrandt suffered substantial damages due to the Defendants' infringement. Furthermore, upon information and belief, such infringement was willful, making this an

exceptional case and entitling Rembrandt to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

**COUNT II: INFRINGEMENT OF U.S. PATENT NO. 5,778,234**

23. Rembrandt refers to and incorporates herein the allegations of Paragraphs 1-17 above.

24. Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 5,778,234, entitled "Method for Downloading Programs" ("the '234 patent.>"). A true copy of the '234 patent is attached as Exhibit B.

25. The '234 patent was duly and legally issued by the United States Patent and Trademark Office on July 7, 1998, after full and fair examination.

26. During the Post-Petition Period, the Defendants have directly or indirectly infringed the '234 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '234 patent, in this district and otherwise within the United States. For example, the Defendants infringed the '234 patent by providing high-speed cable modem internet products and services to subscribers.

27. Rembrandt suffered substantial damages due to the Defendants' infringement. Furthermore, upon information and belief, such infringement was willful, making this an exceptional case and entitling Rembrandt to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

**COUNT III: INFRINGEMENT OF U.S. PATENT NO. 6,131,159**

28. Rembrandt refers to and incorporates herein the allegations of Paragraphs 1-17 above.

29. Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 6,131,159, entitled "System for Downloading Programs" ("the '159 patent."). A true copy of the '159 patent is attached as Exhibit C.

30. The '159 patent was duly and legally issued by the United States Patent and Trademark Office on October 10, 2000, after full and fair examination.

31. During the Post-Petition Period, the Defendants have directly or indirectly infringed the '159 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '159 patent, in this district and otherwise within the United States. For example, the Defendants infringed the '159 patent by providing high-speed cable modem internet products and services to subscribers.

32. Rembrandt suffered substantial damages due to the Defendants' infringement. Furthermore, upon information and belief, such infringement was willful, making this an exceptional case and entitling Rembrandt to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

**COUNT IV: INFRINGEMENT OF U.S. PATENT NO. 6,950,444**

33. Rembrandt refers to and incorporates herein the allegations of Paragraphs 1-17 above.

34. Rembrandt is the owner of all right, title and interest, including the right to sue, enforce and recover damages for all infringements, in U.S. Patent No. 6,950,444, entitled "System and Method for a Robust Preamble and Transmission Delimiting in a Switched-Carrier Transceiver" ("the '444 patent."). A true copy of the '444 patent is attached as Exhibit D.

35. The '444 patent was duly and legally issued by the United States Patent and Trademark Office on September 27, 2005, after full and fair examination.

36. During the Post-Petition Period, Defendants directly or indirectly infringed the '444 patent by practicing or causing others to practice, by inducement or contributorily, the inventions claimed in the '444 patent, in this district and otherwise within the United States. For example, the Defendants infringed the '444 patent by providing high-speed cable modem internet products and services to subscribers.

37. Rembrandt suffered substantial damages due to the Defendants' infringement. Furthermore, upon information and belief, such infringement was willful, making this an exceptional case and entitling Rembrandt to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

#### **PRAYER FOR RELIEF**

WHEREFORE, Rembrandt prays that it have judgment from the District Court against the Defendants for the following:

- (1) An order that the Defendants have infringed the patents-in-suit;
- (2) An award of damages for said infringement;
- (4) An award of increased damages pursuant to 35 U.S.C. § 284;
- (5) An award of all costs of this action, including attorneys' fees and interest; and
- (6) Such other and further relief, at law or in equity, to which Rembrandt is justly entitled.

Dated: September 13, 2006.

**SUSMAN GODFREY L.L.P.**

By: /s/ Vineet Bhatia

VINEET BHATIA (VB 9964)

MAX L. TRIBBLE, JR.

Texas Bar 20213950 (*application pending*)

EDGAR SARGENT

Washington Bar 28283 (*application pending*)

BROOKE A.M. TAYLOR

Washington Bar 33190 (*application pending*)

TIBOR L. NAGY

Texas Bar 24041562 (*application pending*)

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**Exhibit A**



US005710761A

**United States Patent** [19]

Scott

[11] Patent Number: **5,710,761**[45] Date of Patent: **Jan. 20, 1998**[54] **ERROR CONTROL NEGOTIATION BASED ON MODULATION**5,530,881 8/1996 Siddhar et al. 375/222  
5,636,037 6/1997 Saitoh 375/222

[75] Inventor: Robert Earl Scott, Indian Rocks Beach, Fla.

Primary Examiner—Melvin Marcelo  
Attorney, Agent, or Firm—Thomas, Kayden, Horstemeier & Riskey

[73] Assignee: Paradyne Corporation, Largo, Fla.

[57] **ABSTRACT**

[21] Appl. No.: 458,848

[22] Filed: May 31, 1993

[51] Int. Cl.<sup>6</sup> H04L 1/00

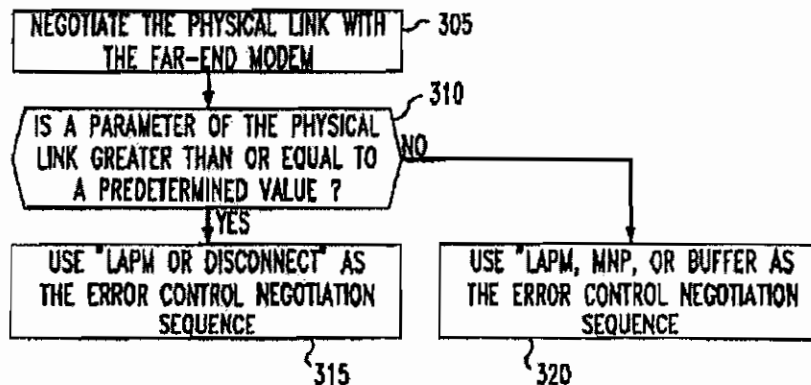
[52] U.S. Cl. 378/252; 375/222; 379/93.08

[58] Field of Search 370/252, 465, 370/466, 467, 469; 375/222; 379/93

[56] **References Cited****U.S. PATENT DOCUMENTS**4,713,044 12/1987 Gertner 375/8  
5,384,780 1/1995 Lomp et al. 375/222  
5,430,793 7/1995 Uetinen et al. 375/222  
5,481,696 1/1996 Lomp et al. 395/500

A modem dynamically selects the type of error-control negotiation sequence as a function of a negotiated parameter of the physical layer. In one embodiment of the invention, a modem selects between error-control negotiation sequences as a function of the type of modulation negotiated in the physical layer. In particular, the modem has at least two type of error-control negotiation sequences to select from: "LAPM or Disconnect," and "LAPM, MNP or Buffer." When the modem negotiates a V.32 or higher modulation, the modem uses the "LAPM or Disconnect" error control negotiation sequence. However, when the modem negotiates a V.22 bis or lower modulation, the modem uses the "LAPM, MNP or Buffer" error control sequence.

16 Claims, 1 Drawing Sheet



U.S. Patent

Jan. 20, 1998

5,710,761

FIG. 1

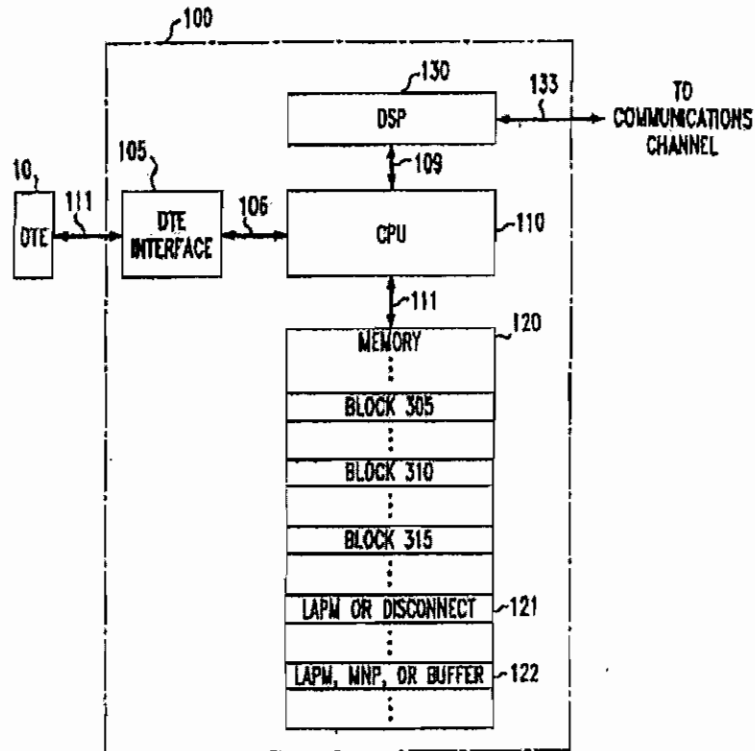
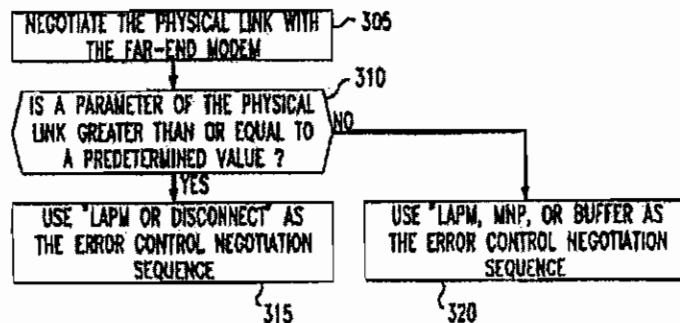


FIG. 2



5,710,761

# 1 ERROR CONTROL NEGOTIATION BASED ON MODULATION

## BACKGROUND OF THE INVENTION

The present invention relates to data communications equipment, e.g., modems, and, more particularly, to the error control negotiation phase of establishing a data connection.

In establishing a data connection between two modems, the modems perform a "handshaking" sequence to negotiate various parameters about the data connection, e.g., the type of modulation (which relates to line speed), and the type of error control protocol. The type of modulation is representative of the "physical" layer of a data connection, while the type of error control protocol is representative of the "link" layer of the data connection. The negotiation of the physical layer is always negotiated before the link layer.

The types of error control protocols used today are: "Link Access Protocol Modem" (LAPM), "Microcom Networking Protocol" (MNP), or "Buffer" (which in reality is no error control). Typically, in negotiating the type of error control protocol a modem tries each type of error control protocol in turn. In particular, the modem uses a negotiation sequence defined herein as "LAPM, MNP, or Buffer." In this negotiation sequence, the modem attempts to connect with the far-end modem for several seconds, e.g., 2 seconds, using an "LAPM" protocol like International Telecommunication Union (ITU) standard V.42. If the far-end modem does not appropriately respond, the modem then tries to connect with the far-end modem for several seconds, e.g., 6 seconds, using the "MNP" protocol. If this too is unsuccessful, the modem then falls back to a non-error control mode, i.e., the "Buffer" mode of operation. This type of negotiation sequence typically allows a modem to connect to the widest range of industry-available modems.

Unfortunately with higher modulation speeds available, like those in ITU standards V.34 and, to a lesser degree, V.32bis, the above error control negotiation sequence can present a problem. In particular, as noted above, the negotiation of the line speed (modulation) occurs before the negotiation of the type of error control. In order to determine the appropriate line speed, a modem uses a technique called "line probing." Unfortunately, the accuracy of current line probing techniques is not perfect. As a result, a modem may erroneously connect at too high a line speed. In other words, even though the line speed was successfully negotiated, the error rate at that line speed is high. This affects the time it takes to perform the subsequent error control negotiation. In particular, with an increase in the error rate, the LAPM type of error control may not be negotiated within the 2 seconds, mentioned above. Further, in severe cases, the time delay in negotiating the error control protocol will be so long that neither LAPM nor MNP is negotiated, causing the modem to fallback to buffer mode. The latter presents a problem, since users typically want V.42 error control and V.42bis data compression for their data calls, however in buffer mode neither V.42 error control nor V.42bis data compression are available.

One way to solve the above-mentioned problem is to have a different negotiation sequence for error control negotiation—"LAPM or Disconnect" for example. With this negotiation setting, the modem tries for an extended length of time, e.g., 30 seconds, to negotiate a LAPM data connection. Even if the modem has trouble at the start of the call, LAPM may still be negotiated because of the longer time delay. However, this negotiation sequence presents a problem when connecting to modems that do not support

LAPM, i.e., MNP-only or non-error-control modems. In order to connect to MNP-only or non-error-control modems, the user must switch the modem back to using the "LAPM, MNP, or Buffer" error control negotiation sequence, described above. Typically, the user switches between error control negotiation sequences via an respective AT command. This is not user-friendly. In today's marketplace, the configuration of the modem itself, e.g., what type of error control negotiation sequence to use, should be transparent to the user.

## SUMMARY OF THE INVENTION

However, I have realized a solution that solves all of the above problems and is user-friendly. I have observed that almost every high-speed modem (V.34, V.32bis, V.32) has a LAPM mode, and that the LAPM mode is enabled. Further, only the low-speed modems (V.22bis or below) are MNP-only or non-error control. And, finally, the modulation (physical layer) is always negotiated before the error control protocol (link layer). Therefore, and in accordance with the invention, a modem dynamically selects the type of link layer negotiation sequence as a function of a negotiated parameter of the physical layer.

In one embodiment of the invention, a modem selects between error control negotiation sequences as a function of the type of modulation negotiated in the physical layer. In particular, the modem has at least two type of error control negotiation sequences to select from: "LAPM or Disconnect," and "LAPM, MNP or Buffer." When the modem negotiates a V.32 or higher modulation, the modem uses the "LAPM or Disconnect" error control negotiation sequence. However, when the modem negotiates a V.22bis or lower modulation, the modem uses the "LAPM, MNP or Buffer" error control sequence.

In another embodiment of the invention, a modem uses the data rate negotiated at the physical layer, rather than the modulation, to select the type of error control sequence. For example, if the modem connects at 2400 bits per second (bps) or below, the modem uses the "LAPM, MNP or Buffer" error control sequence. However, if the modem connects at a rate higher than 2400 bps, the modem uses the "LAPM or Disconnect" error control negotiation sequence. It should be noted that even though V.34 supports 2400 bps, I have observed that this data rate is unlikely to be used, i.e., a data rate of 2400 bps or less can be used to infer there is no high-speed modem in the data connection.

The above-described inventive concept provides a number of advantages. The user does not have to administer the modem to select a particular type of error control negotiation sequence via an AT command or other type of setup setting. Further, a modem incorporating the inventive concept still maintains compatibility with a large part of the currently installed-base of modems. Finally, this approach allows a high-speed modem to connect at the highest feasible rate and still negotiate the use of the LAPM protocol.

## BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a block diagram of a data communications equipment embodying the principles of the invention; and  
FIG. 2 is a flow diagram of an illustrative method embodying the principles of the invention for use in the modem of FIG. 1.

## DETAILED DESCRIPTION

FIG. 1 shows an illustrative high-level block diagram of a modem embodying the principles of the invention. As

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shows, modem 100 couples to a communications channel (not shown) via line 133, which is, e.g., a local loop that couples modem 100 to a local central office (not shown). Modem 100 is also coupled to respective data terminal equipment (DTE) 10 via line 11. Other than the inventive concept, the components of modem 100 are well-known and will not be described in detail. Modem 100 includes DTE interface 105, microprocessor-based central processing unit (CPU) 110, memory 120 and digital signal processing circuitry (DSP) 130. Since FIG. 1 is a high-level block diagram, other parts of modem 100 not important to the inventive concept are assumed to be included within these representative components. For example, DSP 130 is representative of not only a digital signal processing chip, but also includes the "data access arrangement" (DAA) circuitry that couples any transmitted and received data signals to, and from, line 133. Further, although shown as single lines in FIG. 1, lines 11, 106, 111, 109, and 123, are representative of a plurality of signals as known in the art to interconnect the various components. For example, line 11 is representative of any one of a number of ways for coupling data communications equipment to data terminal equipment, e.g., a serial interface like that specified in Electronic Industry Association (EIA) standard RS-232.

As known in the art, CPU 110 provides a controlling function for modem 100, e.g., CPU 110 controls, via line 109, DSP 130 for establishing, maintaining, and disconnecting, from a data connection to a far-end modem (not shown), via line 109. In performing this controlling function, CPU 110 operates on, or executes, program data stored in memory 120 via line 111, which is representative of control, address, and data signals (not shown).

In accordance with the inventive concept, modem 100 dynamically selects the type of error control negotiation sequence as a function of the type of physical layer negotiated. Turning now to FIG. 2, an illustrative method embodying the principles of the invention will be described. The steps shown in FIG. 2 are illustratively stored in memory 120 as program data as represented by blocks 305, block 310, block 315, etc., of FIG. 1, respectively. For the purposes of this description, it is assumed that modem 100 has already initiated a data call to a far-end modem (not shown) and a handshaking sequence has begun. As known in the art, CPU 110 first negotiates with the far-end modem the physical layer of the data connection, as shown in step 305. (It should be realized that since this is a negotiation process, whether modem 100 is the originating, or answering, modem is irrelevant to the inventive concept). During the physical layer negotiation, modem 100 negotiates the type of modulation, e.g., V.22, V.22bis, V.32, V.32bis, and V.34 industry standards. After negotiation of the physical layer, CPU 110 evaluates a negotiated parameter of the physical layer in step 310. In particular, CPU 110 compares a value of the negotiated parameter to a predefined value. If the value of the negotiated parameter is greater than or equal to the predefined value, CPU 110 uses an "LAPM or Disconnect" error control negotiation sequence in step 315 as part of the link layer negotiation. The software instructions for executing the "LAPM or Disconnect" error control negotiation sequence are illustratively stored in memory 120 at location 121. With this negotiation setting, modem 100 tries for an extended length of time to negotiate a LAPM link layer on the data connection. If a LAPM link layer cannot be negotiated, modem 100 disconnects.

On the other hand, if the value of the negotiated parameter is less than the predefined value, CPU 110 uses an "LAPM, MNP or Buffer" error control negotiation sequence in step

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320 as part of the link layer negotiation. The software instructions for executing the "LAPM, MNP, or Buffer" error control negotiation sequence are illustratively stored in memory 120 at location 122. As described earlier, in this negotiation sequence modem 100 attempts to connect with the far-end modem for several seconds using an "LAPM" protocol like International Telecommunication Union (ITU) standard V.42. If the far-end modem does not appropriately respond, modem 100 then tries to connect with the far-end modem for several seconds using the "MNP" protocol. If this too is unsuccessful, modem 100 then falls back to a non-error control mode, i.e., the "Buffer" mode of operation.

In one embodiment of the invention, the negotiated parameter from the physical layer is the type of modulation negotiated in the physical layer. In particular, when modem 100 negotiates a V.32 or higher modulation, modem 100 performs step 315, described above. However, when modem 100 negotiates a V.22bis or lower modulation, modem 100 performs step 320, described above.

In another embodiment of the invention, the negotiated parameter from the physical layer is the negotiated data rate. For example, if modem connects below 4800 bps, modem 100 performs step 320, described above. However, when modem 100 connects at a rate equal to or higher than 4800 bps, modem 100 performs step 315, described above. It should be noted that even though high-speed modulations, like V.34, support rates below 4800, I have observed that these data rates are unlikely to be used. As a result, a data rate less than 4800 bps can be used to infer there is no high-speed modem in the data connection.

The above-described inventive concept provides a number of advantages. The user does not have to administer the modem to select a particular type of error control negotiation sequence for use during the link layer negotiation. Further, a modem incorporating the inventive concept still maintains compatibility with a large part of the currently installed base of modems. Finally, this approach allows a high-speed modem to connect at the highest feasible rate and still negotiate the use of the LAPM protocol.

The foregoing merely illustrates the principles of the invention and it will thus be appreciated that those skilled in the art will be able to devise numerous alternative arrangements which, although not explicitly described herein, embody the principles of the invention and are within its spirit and scope.

For example, although the invention is illustrated herein as being implemented with discrete functional building blocks, e.g., a memory, CPU, etc., the functions of any one or more of these building blocks can be carried out using one or more appropriate integrated circuits, e.g., a microprocessor that includes memory.

In addition, although described in the context of a modem external to the data terminal equipment, the inventive concept applies to any other forms of coupling a modem to data terminal equipment, e.g., a modem that is internal to a personal computer or a modem that is part of a mobile phone transceiver. Finally, the selection of a link layer negotiation sequence can be a function of other data rates, types of modulations, and/or other parameters of the physical layer.

What is claimed:

1. A method for use in data communications equipment, the method comprising the steps of:

negotiating a physical layer of a data connection with a far-end data communications equipment to determine a set of parameters for the physical layer of the data connection with the far-end data communications equipment; and

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selecting one of a number of error control negotiation sequences as a function of a value of at least one parameter from the set of parameters for the physical layer.

2. The method of claim 1, further including the step of negotiating error control of the data connection with the far-end data communications equipment in accordance with the selected one of the number of error control negotiation sequences.

3. The method of claim 1, wherein the at least one parameter is the type of modulation negotiated with the far-end data communications equipment.

4. The method of claim 3, wherein the number of error control negotiation sequences include a Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence and a Link Access Protocol Modem or Disconnect sequence.

5. The method of claim 4, wherein the Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence is selected when the type of modulation negotiated is less than V32, and wherein the Link Access Protocol Modem or Disconnect sequence is selected when the type of modulation negotiated is greater than or equal to V32.

6. The method of claim 1, wherein the at least one parameter is the data rate negotiated with the far-end data communications equipment.

7. The method of claim 6, wherein the number of error control negotiation sequences include a Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence and a Link Access Protocol Modem or Disconnect sequence.

8. The method of claim 7, wherein the Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence is selected when the data rate is less than 4800 bits per second, and wherein the Link Access Protocol Modem or Disconnect sequence is selected the data rate is greater than or equal to 4800 bits per second.

9. Data communications apparatus comprising:

a memory that stores a number of error control negotiation sequences; and

processor circuitry that negotiates a physical layer of a data connection with a far-end data communications equipment to determine a set of parameters for the

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physical layer of the data connection with the far-end data communications equipment, and then selects from memory one of a number of error control negotiation sequences as a function of a value of at least one parameter from the set of parameters for the physical layer.

10. The apparatus of claim 9, wherein the processor negotiates error control of the data connection with the far-end data communications equipment in accordance with the selected one of the number of error control negotiation sequences.

11. The apparatus of claim 9, wherein the at least one parameter is the type of modulation negotiated with the far-end data communications equipment.

12. The apparatus of claim 11, wherein the number of error control negotiation sequences include a Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence and a Link Access Protocol Modem or Disconnect sequence.

13. The apparatus of claim 12, wherein the processor selects the Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence when the type of modulation negotiated is less than V32, and wherein the processor selects the Link Access Protocol Modem or Disconnect sequence when the type of modulation negotiated is greater than or equal to V32.

14. The apparatus of claim 9, wherein the at least one parameter is data rate negotiated with the far-end data communications equipment.

15. The apparatus of claim 9, wherein the number of error control negotiation sequences include a Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence and a Link Access Protocol Modem or Disconnect sequence.

16. The apparatus of claim 15, wherein the processor selects the Link Access Protocol Modem, Microcom Networking Protocol, or Buffer sequence when the data rate is less than 4800 bits per second, and wherein the processor selects the Link Access Protocol Modem or Disconnect sequence when the data rate is greater than or equal to 4800 bits per second.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,710,761  
DATED : January 20, 1998  
INVENTOR(S) : Scott

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page of the patent, second column, six lines under the heading "ABSTRACT", change "type" to --types--.  
Column 2, line 27, after "at least two" change "type" to --types--.  
Column 4, line 22, change "4800" (in bold) to --4800-- (in regular font).  
Column 4, line 49, after "can be" delete "carded" and insert therefor --carried--.

Signed and Sealed this  
Twenty-sixth Day of May, 1998

Attest:



BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

**Exhibit B**



US005778234A

**United States Patent** [19]

Hecht et al.

[11] Patent Number: **5,778,234**[45] Date of Patent: **Jul. 7, 1998**[54] **METHOD FOR DOWNLOADING PROGRAMS**

[75] Inventors: Gideon Hecht, Scranton; Kurt Ervin Bokanquist, Largo; Donald C. Snell, Clearwater, all of Fla.

[73] Assignee: Paradyne Corporation, Largo, Fla.

[21] Appl. No.: 899,834

[22] Filed: Jul. 24, 1997

**Related U.S. Application Data**

[62] Division of Ser. No. 880,237, May 8, 1992.

[51] Int. Cl.<sup>6</sup> G06F 9/44

[52] U.S. CL. 395/772; 395/652

[58] Field of Search 395/712, 651, 395/652

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*IBM Technical Disclosure Bulletin*, vol. 34, No. 3, Aug. 1991, Armonk, NY, US pp. 286-289.

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Assistant Examiner—Kakali Chaki

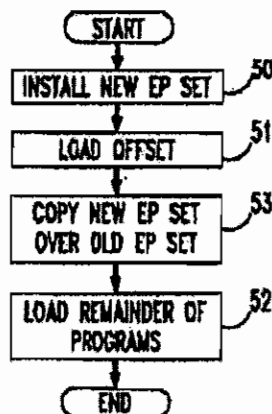
Attorney, Agent, or Firm—Thomas, Kayden, Horstmeier &amp; Risley LLP

[57]

**ABSTRACT**

A modified version of the operating communication program of a stored program controlled apparatus is downloaded by first downloading a segment of the new package of programs which contains the essential portion of the new programs. Control of the apparatus is then transferred to the new program segment. Thereafter, utilizing the downloaded essential portion of the new package of programs, the remainder of the new package of programs is downloaded.

8 Claims, 1 Drawing Sheet



U.S. Patent

Jul. 7, 1998

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FIG. 1

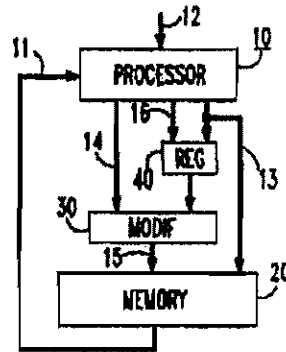


FIG. 2

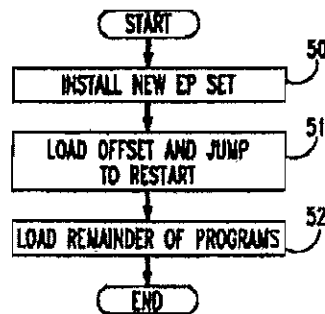
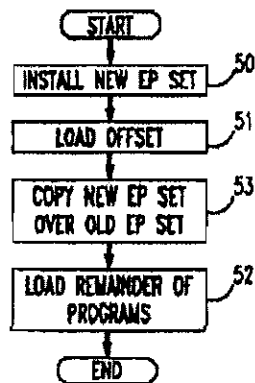


FIG. 3



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# 1 METHOD FOR DOWNLOADING PROGRAMS

This application is a division of U.S. patent application having Ser. No. 07/880,257 of Hecht, et al., filed May 8, 1992.

## BACKGROUND OF THE INVENTION

This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of programs.

Stored program controlled apparatus can conveniently be divided into two types; one where the stored programs are completely unalterable under normal operating circumstances, and the other where the stored programs are alterable, at least at times, during normal operation. In apparatus of the first type, the program is often executed automatically and the user does not even know that the controlled apparatus is "stored program controlled". This is typically the case in equipment that is designed for people who are not knowledgeable in computers and for whom the equipment is just a tool of the trade. "Point of sale" terminals, such as check-out terminals at a supermarket, are a good example. Modems are another example. People who use this equipment desire fail-safe operation and they do not want to be bothered with loading programs, fixing program bugs, installing updated versions of software, etc.

One approach to programming such equipment is to imprint the program into read-only-memory integrated circuits and physically install the circuits into the equipment. The problem with this approach is that updated versions of the program require the creation of new sets of read-only memories and new installations.

When a communication link is present, "downloading" the programs to the equipment from a remote processor, through the communication link, forms another approach for programming the equipment. It has been known in the art for some time that it is feasible to download limited types of control information from a remote processor. It is also known to download entire machine language application programs. Often such equipment does not include writable non-volatile store, such as a hard disk, so the programs are stored in battery protected read/write memories.

This is an unattractive solution because it leaves a substantial portion of program memory to be at risk. To mitigate this problem, U.S. Pat. No. 4,724,521, suggests storing within read-only memories of the local equipment a number of general purpose routines which comprise instructions to be executed by the central processing unit to accomplish a particular program task. These, in effect, form a set of macro-instructions. The downloaded machine language program utilizes these macro-instructions to the extent possible, and thereby achieves flexibility without the need to download substantial amounts of program code.

In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents is not changed. That resident portion contains "boot-up" segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set. This set of programs should, of course, be a non-volatile store because there is always a possibility of power loss.

The fact that the EP set is needed to maintain communications presents a problem when the EP set itself needs to be

modified or updated. Indeed, that is often the case with modems, where essentially the sole function of the modem software is to support communication.

## SUMMARY OF THE INVENTION

The problem of downloading a modified version of the operating communication program, and the problem of effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory. The start address specification means stores information that is downloaded through the communication link, and that information is used in defining the address from where the communication link programs are initiated.

In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address. Utilizing the most recently downloaded EP set of the new communication package, the second segment downloads the remainder of the new package.

## BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 presents a block diagram of an arrangement for carrying out this invention;

FIG. 2 is a flow diagram of a downloading process in accordance with this invention; and

FIG. 3 is a flow diagram of an augmented downloading process in accordance with this invention.

## DETAILED DESCRIPTION

A modem's primary function is to enable communications between a customer's digital equipment and a remote apparatus over a transmission medium. In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem. These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs—including the EP set of programs that carry out the elemental communications—are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile "boot-up" read-only-memory. All programs (including the boot-up programs) can be stored in a single memory arrangement which, for some applications, can consist of just two memory devices.

FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively. In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20. Modifier 30 is responsive to

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register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20. A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing.

It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory. It should also be understood, and noted, that although this invention is described in connection with modems, its principles are applicable to all stored program apparatus. In particular, the principles of this invention are applicable to all situations where it is desirable to download an entire set of new programs, including the EP set. For example, this invention is useful in PCs, "point of sale" terminals, etc.

The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30.

The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending information out on line 12 and for receiving information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere.

The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set.

In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP

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set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20.

After the new EP set is installed in memory locations X through X+N, where X is the offset address (X=M/2, for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address.

The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M).

It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Memory 20 must also be relatively fast because it directly affects the processing speed that can be attained with the FIG. 1 arrangement. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20. This memory must be erased in bulk before new information can be written in it. To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct chips (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves.

To summarize the downloading process of this invention,

1. Bulk erase the half of memory 20 which does NOT contain the EP set of programs;
2. download a new EP set of programs to the erased half of memory 20;
3. download the offset address to pass control to the new EP set of programs;
4. bulk erase the other half of memory 20;
5. download the remainder of programs into memory 20.

If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can be manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10.

Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20):

1. Bulk erase the second half of memory 20;

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2. download a new EP set of programs to the second half of memory 20;  
 4. download the offset address to pass control to the new EP set of programs;  
 5. bulk erase the first half of memory 20;  
 6. copy the contents of the second half of memory 20 into the first half of memory 20;  
 7. reset the offset address to 0; and  
 8. download the remainder of programs into memory 20.

Admittedly, during the copy sequence (which may also be a "move" sequence) the arrangement is vulnerable to power failures. Since the time of copying or moving is very small, this is a very unlikely event. Still, to protect against this unlikely event, the power source can be designed to have sufficient reserve to complete the copy operation, or to protect the starting address. A capacitor at the output of the power supply may supply the necessary power reserve.

In the arrangement described above where memory 20 consists of two FLASH EPROM chips, register 40 needs to have only one bit of memory, and modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active.

We claim:

1. A method for installing a new set of communication programs  $P_{new}$  into a stored program controlled apparatus that includes a communication port and a memory by transmitting said set of programs  $P_{new}$  to said apparatus via said port, with the aid of a set of communications programs  $P_{old}$  already resident in said memory, where said set of programs  $P_{old}$  contains a subset of programs  $EP_{old}$  that occupy less than half of the memory and said set of programs  $P_{new}$  also contains a subset of programs  $EP_{new}$  that, when installed, occupy less than half of the memory,

comprising the steps of:  
 installing the  $EP_{new}$  programs in a first area of said memory that contains programs other than the  $EP_{old}$  programs, thereby overwriting at least a portion of one program in said  $P_{old}$  set of programs;

altering operation of said apparatus to execute the  $EP_{new}$  programs instead of the  $EP_{old}$  programs; and

installing the remaining programs of said  $P_{new}$  set of programs in a second area of said memory, said second area constituting memory locations not occupied by the  $EP_{new}$  programs.

2. The method of claim 1 further comprising

a step of moving, interposed between said step of altering operation of the apparatus and said step of installing the remaining programs, that installs said  $EP_{new}$  programs into memory locations starting at a location that corresponds to a starting location of the  $EP_{old}$  programs, and

a second step of altering operation of said apparatus to execute the  $EP_{new}$  programs in the installed locations by said step of moving.

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wherein said installing the remaining programs of said  $P_{new}$  set of programs stores the programs in memory locations not occupied with the  $EP_{new}$  programs installed by said step of moving.

3. The method of claim 1, further comprising the steps of: erasing said first area of said memory, said erasing step to be performed prior to said step of installing the  $EP_{new}$  programs into said first area of said memory; and

erasing said second area of said memory, said erasing step to be performed after said step of altering operation of the apparatus and prior to said step of installing the remaining programs of said  $P_{new}$  set of programs.

4. The method of claim 1, wherein said step of altering operation of said apparatus to execute said  $EP_{new}$  programs is accomplished by installing an offset address to pass control of said apparatus to said  $EP_{new}$  programs.

5. A method for installing a new set of communication programs  $P_{new}$  into a stored program controlled apparatus that includes a communication port and a memory by transmitting said set of programs  $P_{new}$  to said apparatus via said port, with the aid of a set of communications programs  $P_{old}$  already resident in said memory, where said set of programs  $P_{old}$  contains a subset of programs  $EP_{old}$  that occupy less than half of the memory and said set of programs  $P_{new}$  also contains a subset of programs  $EP_{new}$  that, when installed, occupy less than half of the memory, comprising the steps of:

installing the  $EP_{new}$  programs in a first area of said memory that contains programs other than the  $EP_{old}$  programs, thereby overwriting at least a portion of one program in said  $P_{old}$  set of programs;

altering operation of said apparatus to execute the  $EP_{new}$  programs instead of the  $EP_{old}$  programs;

moving the  $EP_{new}$  programs from said first area of memory to a second area of said memory; and

installing the remaining programs of said  $P_{new}$  set of programs in said first area of memory.

6. The method of claim 5, further comprising the step of: erasing said first area of said memory, said erasing step to be performed prior to said step of installing the  $EP_{new}$  programs into said first area of said memory.

7. The method of claim 5, wherein said moving step further comprises the steps of:

copying the  $EP_{new}$  programs from said first area of memory to said second area of memory; and

erasing said first area of memory.

8. The method of claim 5, wherein said step of altering operation of said apparatus to execute said  $EP_{new}$  programs is accomplished by installing an offset address to pass control of said apparatus to said  $EP_{new}$  programs.

• • • • •

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,778,234  
DATED : July 7, 1998  
INVENTOR(S) : Hecht, *et al.*

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 4, line 45, delete "that".

In column 5, line 48, insert ":" after "comprising".

In column 6, line 1, insert "step of" after the first appearance of "said" and before "installing".

Signed and Sealed this  
Seventeenth Day of November, 1998

Attest:



BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

**Exhibit C**



US006131159A

**United States Patent** [19]

Hecht et al.

[11] Patent Number: **6,131,159**[45] Date of Patent: **Oct. 10, 2000**[54] **SYSTEM FOR DOWNLOADING PROGRAMS**

[75] Inventors: Gideon Hecht, Seminole; Kurt Ervin Holmquist, Largo; Donald C. Snell, Clearwater, all of Fla.

[73] Assignee: Paradyne Corporation, Largo, Fla.

[21] Appl. No.: 07/880,257

[22] Filed: May 8, 1992

[51] Int. Cl.<sup>7</sup> G06F 9/445

[52] U.S. Cl. 713/1; 713/100; 711/1

[58] Field of Search 395/700, 651, 395/652, 653, 712; 364/DIG. 1, DIG. 2; 713/1, 2, 100; 711/114, 1, 145, 202-206; 710/23, 104

[56] **References Cited****U.S. PATENT DOCUMENTS**

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 2 227 584 8/1990 United Kingdom G06F 12/12

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Electronic Engineering, vol. 64, No. 783, "SGS-Thomson Block Erase Flash in 16 Bit RISC Controller", Mar. 1992, Woolrich, London, GB, p. 83.

IBM Technical Disclosure Bulletin, vol. 34, No. 3, Aug. 1991, Armonk, NY, US, pp. 286-289.

Primary Examiner—Thomas C. Lee

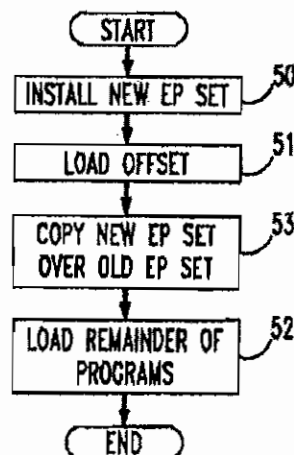
Assistant Examiner—Rijue Mai

Attorney, Agent, or Firm—Thomas, Kayden, Horstemeier & Risley LLP

[57] **ABSTRACT**

A modified version of the operating communication program of a stored program controlled apparatus is installed with the aid of a downloadable start address specification means, optionally realized with an EEPROM memory. The start address specification means stores information that is downloaded through a communication port in the apparatus, and that information is used in defining the address from where the communication programs are initiated. In accordance with the method of this invention, downloading of the entire new set of programs is effected by first downloading a segment of the essential portion of the new package of programs. Control is then transferred to the new segment by downloading appropriate information into the start address specification means. Thereafter, utilizing the downloaded essential portion of the new package of programs, the remainder of the new package is downloaded.

21 Claims, 1 Drawing Sheet



U.S. Patent

Oct. 10, 2000

6,131,159

FIG. 1

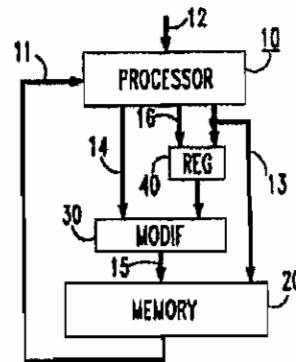


FIG. 2

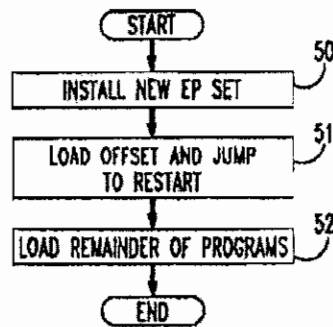
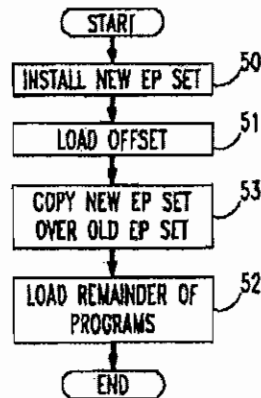


FIG. 3



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## SYSTEM FOR DOWNLOADING PROGRAMS

## BACKGROUND OF THE INVENTION

This invention relates to stored program controlled apparatus and, in particular, to apparatus with a capability for remote updating of its entire set of programs.

Stored program controlled apparatus can conveniently be divided into two types; one where the stored programs are completely unalterable under normal operating circumstances, and the other where the stored programs are alterable, at least at times, during normal operation. In apparatus of the first type, the program is often executed automatically and the user does not even know that the controlled apparatus is "stored program controlled". This is typically the case in equipment that is designed for people who are not knowledgeable in computers and for whom the equipment is just a tool of the trade. "Point of sale" terminals, such as check-out terminals at a supermarket, are a good example. Modems are another example. People who use this equipment desire fail-safe operation and they do not want to be bothered with loading programs, fixing program bugs, installing updated versions of software, etc.

One approach to programming such equipment is to imprint the program into read-only-memory integrated circuits and physically install the circuits into the equipment. The problem with this approach is that updated versions of the program require the creation of new sets of read-only memories and new installations.

When a communication link is present, "downloading" the programs to the equipment from a remote processor, through the communication link, forms another approach for programming the equipment. It has been known in the art for some time that it is feasible to download limited types of control information from a remote processor. It is also known to download entire machine language application programs. Often such equipment does not include writable non-volatile store, such as a hard disk, so the programs are stored in battery protected read/write memories. This is an unattractive solution because it leaves a substantial portion of program memory to be at risk. To mitigate this problem, U.S. Pat. No. 4,724,521, suggests storing within read-only memories of the local equipment a number of general purpose routines which comprise instructions to be executed by the control processing unit to accomplish a particular program task. These, in effect, form a set of macro-instructions. The downloaded machine language program utilizes these macro-instructions to the extent possible, and thereby achieves flexibility without the need to download substantial amounts of program code.

In all of the known approaches, however, there is a program portion in the local equipment that is resident in a read-only memory, and its contents are not changed. That resident portion contains "boot-up" segments and program segments that are necessary to maintain the communication between the remote processor and the local equipment (so that the process of downloading the programs can continue). This set of programs is the "essential programs" (EP) set. This set of programs should, of course, be a non-volatile store because there is always a possibility of power loss.

The fact that the EP set is needed to maintain communications presents a problem when the EP set itself needs to be modified or updated. Indeed, that is often the case with modems, where essentially the sole function of the modem software is to support communication.

## SUMMARY OF THE INVENTION

The problem of downloading a modified version of the operating communication program, and the problem of

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effectively updating the entire set of programs in a stored program controlled apparatus, such as a modem, is solved with a downloadable start address specification means and, optionally, with an EEPROM memory. The start address specification means stores information that is downloaded through the communication link, and that information is used in defining the address from where the communication link programs are initiated.

In accordance with the method of this invention, downloading comprises what may be considered two communication segments. In the first segment the essential portion of the new package (EP set) of programs is downloaded to some chosen location in the local apparatus and the downloadable start address specification means is loaded with the appropriate new start address. Utilizing the most recently downloaded EP set of the new communication package, the second segment downloads the remainder of the new package.

## BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 presents a block diagram of an arrangement for carrying out this invention;

FIG. 2 is a flow diagram of a downloading process in accordance with this invention; and

FIG. 3 is a flow diagram of an augmented downloading process in accordance with this invention.

## DETAILED DESCRIPTION

A modem's primary function is to enable communications between a customer's digital equipment and a remote apparatus over a transmission medium. In a modem with a stored programmed controlled architecture this communication is effected with a set of programs, which includes call establishment programs, link layer protocols with flow control and error recovery functions, and programs that handle and store the communicated data, as well as the modulation and demodulation programs used by the modem. These programs occupy a significant portion of the modem's program memory. In accordance with this invention, all programs—including the EP set of programs that carry out the elemental communications—are downloadable. That is, the apparatus employing the principles of this invention does not need to have a non-volatile "boot-up" read-only-memory. All programs (including the boot-up programs) can be stored in a single memory arrangement which, for some applications, can consist of just two memory blocks.

FIG. 1 depicts one structure that, in conformance with the principles of this invention, enables the downloading of programs to the modem's program memory. FIG. 1 includes a processor element 10 with a port for receiving signals from, and sending signals to, line 12. Processor 10 is also responsive to line 11 data from program memory 20, and it supplies address and data to memory 20 via bus 13 and bus 14, respectively. In a conventional processor structure, bus 14 is connected to an address port of memory 20. In FIG. 1, address modifier 30 is interposed between processor 10 and program memory 20, with bus 15 supplying the address information to memory 20. Modifier 30 is responsive to register 40, which is loaded with bus 13 data when the register is enabled by bus 16. Modifier 30 is a modulo M adder, where M is the size of memory 20. A typical stored program controlled modem also includes a read/write data memory, means for interfacing with the transmission medium, means for interfacing with the local digital equipment, and perhaps other data and control ports. For purposes of this invention, however, these other elements are irrelevant, so they are not included in the drawing.

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It should be understood that line 12 in the FIG. 1 architecture effectively offers a "remote execution" capability to processor 10, in that the programs which are executed by processor 10 are affected by data supplied by line 12. For example, data supplied by line 12 can effect branching to programs that are normally dormant. One such normally dormant program is a program that downloads information to the program memory. It should also be understood, and noted, that although this invention is described in connection with modems, its principles are applicable to all stored program apparatus. In particular, the principles of this invention are applicable to all situations where it is desirable to download an entire set of new programs, including the EP set. For example, this invention is useful in PCs, "point of sale" terminals, etc.

The operation of the FIG. 1 apparatus is quite simple. The processes carried out by the FIG. 1 apparatus are effected by executing a sequence of instructions that the processor receives from program memory 20 via bus 11. In turn, processor 10 determines which instructions are delivered to it by controlling the addresses applied to memory 20 (typically by controlling a "program counter" within processor 10, which is not shown in the FIG.). The primary difference between a conventional microprocessor arrangement and the FIG. 1 arrangement is that the addresses supplied on bus 14 are not the actual addresses that are applied to program memory 20, because of the interposed circuit 30. One might call these addresses "virtual addresses", which are translated into the real addresses by the additive constant applied by register 40 to modifier circuit 30.

The exact structure and organization of the programs executed by the FIG. 1 arrangement is not really relevant to this invention, but it is to be understood that a protocol exists for sending information out on line 12 and for receiving information from line 12. This protocol provides a mechanism for intelligent communication with processor 10, which includes, for example, knowing when the received data is commands or data, and whether to store the received data in memory 20 or elsewhere.

The programs that can be executed by the FIG. 1 arrangement reside throughout memory 20, but the set of programs that is essential to the maintenance of communication with line 12 (the EP set) may, advantageously, occupy a contiguous segment of memory 20 addresses in the range 0 to N. Within that range of addresses there is a subroutine for installing a new EP set.

In accordance with the principles of this invention, the entire set of programs contained in memory 20 can be over-written with a new set of programs (in a process initiated by the apparatus itself or by the party connected to the apparatus via line 12) by following the procedure outlined in FIG. 2. In step 50 of FIG. 2, a command is received on line 12 to branch to the subroutine in the EP set that installs new EP sets (that command may simply be a data word that is installed in a particular read/write memory location). After supplying the branch instruction, the new EP set of programs are downloaded via line 12. Optionally, an offset address that is the starting address of the new EP set (the address corresponding to 0 in the existing EP set) is also downloaded. Alternatively, the offset address may be predefined, in which case it does not need to be supplied by line 12. In any event, the offset address is greater than N and less than M-N. It may be noted that N must be less than M/2, because two EP sets must temporarily coexist in memory 20.

After the new EP set is installed in memory locations X through X+N, where X is the offset address ( $X=M/2$ , for example), memory locations that serve as software-defined registers in the new EP set are populated with data that is

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found in the corresponding software-defined addresses in the active EP set. Thereafter, according to step 51, register 40 is loaded with the offset address.

The immediate effect of loading the offset address into register 40 is to transfer control to the newly installed EP set. That means that the program in the new EP set to which control is transferred, must be at a predetermined logic point so that the communication can continue seamlessly. This minor requirement can be easily accommodated by proper planning of the new EP set. Once operation proceeds under control of the new EP set of programs, according to FIG. 2, step 52 conditions processor 10 to account for the offset present in register 40 and loads the remainder of programs destined for memory 20 in addresses higher than X+N (modulo M).

It is obviously important to protect the information loaded into memory 20 from loss. At the very least, that means that memory 20 must be non-volatile. Currently, we use an electrically bulk erasable, programmable, read-only memory (FLASH EEPROM) to form memory 20. This memory must be erased in bulk before new information can be written in it. To install a new EP in such a memory, it is recalled that the EP set must occupy less than half of memory 20, and that makes it convenient to construct memory 20 from at least two distinct erasable memory blocks (distinct in the sense of being able to erase one and not the other). Each segment of the downloading process begins with a bulk erasure of one of the memory 20 halves.

To summarize the downloading process of this invention,

1. Bulk erase the first half of memory 20 which does NOT contain the EP set of programs;
2. download a new EP set of programs to the erased half of memory 20;
3. download the offset address to pass control to the new EP set of programs;
4. bulk erase the other half of memory 20;
5. download the remainder of programs into memory 20.

If register 40 is to contain the offset address for a substantial time after downloading is accomplished, then its contents must be protected in a manner not unlike that of memory 20. Of course, register 40 can be manufactured together with memory 20 and be an EEPROM. However, that is not absolutely necessary, and manufacturing costs could benefit if register 40 were constructed as part of the read/write memory or as part of processor 10.

Register 40 may be a volatile memory if the downloading process is carried out as depicted in FIG. 3. Specifically, by including a copy subroutine in the EP set of programs, the downloading process can be modified to the following (assuming the EP set is in the first half of memory 20):

1. Bulk erase the second half of memory 20;
2. download a new EP set of programs to the second half of memory 20;
4. download the offset address to pass control to the new EP set of programs;
5. bulk erase the first half of memory 20;
6. copy the contents of the second half of memory 20 into the first half of memory 20;
7. reset the offset address to 0; and
8. download the remainder of programs into memory 20.

Admittedly, during the copy sequence (which may also be a "move" sequence) the arrangement is vulnerable to power failures. Since the time of copying or moving is very small, this is a very unlikely event. Still, to protect against this unlikely event, the power source can be designed to have sufficient reserve to complete the copy operation, or to protect the starting address. A capacitor at the output of the power supply may supply the necessary power reserve.

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In the arrangement described above where memory 20 consists of two FLASH EEPROM chips, register 40 needs to have only one bit of memory, and modifier circuit 30 can be merely an Exclusive OR gate which, with the aid of the one bit memory of register 40, selects the bank of memory that is active.

What is claimed is:

1. A system comprising:
  - (a) a processor;
  - (b) a memory, and a set of programs stored in said memory that are executed when the system needs to be initialized, said memory being of a type which may be completely updated in its entirety but which is not volatile, said memory being the only program memory in said system; and
  - (c) alterable storage means for holding a displacement multi-bit memory address that is used to point to the starting address accessed by the processor when initializing.
2. The system of claim 1 wherein said memory is an EEPROM memory.
3. The system of claim 1 wherein said memory consists of 2-FLASH EEPROM devices.
4. The system of claim 1 wherein said alterable storage means is an EEPROM memory.
5. The system of claim 1 further comprising translation means interposed between said alterable storage means and said memory, wherein said alterable storage means holds an address that translates between addresses directed to the memory via said translation means and addresses actually applied to the memory by said translation means.
6. A system comprising:
  - (a) a processor;
  - (b) a memory coupled to said processor, said memory being the only program memory in the system, said memory being completely updatable in its entirety but non-volatile, there being a set of programs stored in said memory that are executed when the system needs to be initialized; and
  - (c) alterable memory means for storing a multi-bit memory address that controls the starting address accessed by the processor when initializing.
7. The system of claim 6 further comprising means for receiving a trigger signal at a telecommunications input port of the system to begin execution of said programs.
8. A system comprising:
  - (a) a processor;
  - (b) a memory and a communications port coupled to said processor, said communications port being adapted to communicate with devices which are external to said system, said memory being completely updatable in its entirety but non-volatile;
  - (c) a program module in said memory that, when activated by said processor, effects communication with said port; and
  - (d) operationally alterable means for setting the starting address of said program, which address is supplied to said system via said communication port.
9. The system of claim 8 wherein:
  - (a) said memory contains a first set of programs and a second set of programs;
  - (b) said memory is at least twice the size of the size of the first set of programs; and

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- (c) said operationally alterable means sets the starting position of the program executed by said processor in connection with communication with said port at a second specified location that is M removed from the first location, M being half the size of said memory.
10. A system comprising:
  - (a) a processor;
  - (b) a communication port coupled to said processor, said communication port being adapted to communicate with devices which are external to said system;
  - (c) a memory coupled to said processor, said memory being non-volatile and capable of being completely updated in its entirety, said memory containing programs, including a set of programs that are executed when the system needs to be initialized and a program for controlling communication through said communication port; and
  - (d) means for activating said program for controlling communication and receiving information through said communication port to modify the programs in said memory, said information including the program for controlling communication through said communication port and a command that is executed by said processor effectively when it is received.
11. The system of claim 10 wherein the communication port is a telecommunication port.
12. The system of claim 10 wherein the communication port is a telecommunication port and the programs execute the functions of a modem.
13. The system of claim 10 where the communication port receives commands to be executed by the processor and data to be stored in the memory.
14. The system of claim 10 wherein said means for receiving includes means for altering the program according to the information obtained by the means for receiving.
15. The system of claim 10 wherein said means for receiving modifies the programs by altering a portion of the memory contents pursuant to data received via said communication port.
16. The system of claim 10 wherein said means for receiving modifies the programs by replacing them with program data received via said communication port.
17. The system of claim 10 where the means for altering alters all of the programs in the system in a single communication session with said communication port.
18. A system comprising:
  - (a) a processor;
  - (b) a memory coupled to said processor, said memory being of a type, which is completely updatable in its entirety but non-volatile;
  - (c) a set of program means stored in said memory that are activated when said system needs to be updated with a new set of programs; and
  - (d) alterable storage means for holding an offset memory address that is used to point to a starting address accessed by said processor when initializing.
19. The system of claim 18 wherein said memory is an EEPROM memory.
20. The system of claim 18 wherein said memory consists of 2 FLASH EEPROM devices.
21. The system of claim 18 wherein said alterable storage means is an EEPROM memory.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,131,159  
DATED : October 10, 2000  
INVENTOR(S) : Hecht, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4, line 40, insert "be" between "can" and "manufactured".

Column 6, line 49, delete ",", after "type".

Column 6, line 52, change "wit" to --with--.

Signed and Sealed this  
Twenty-fourth Day of April, 2001

Attest:



NICHOLAS P. GOBICI

Attesting Officer

Acting Director of the United States Patent and Trademark Office

## **Exhibit D**



US006950444B1

(12) **United States Patent**  
**Holmquist et al.**

(10) Patent No.: **US 6,950,444 B1**  
 (45) Date of Patent: **Sep. 27, 2005**

(54) **SYSTEM AND METHOD FOR A ROBUST PREAMBLE AND TRANSMISSION DELIMITING IN A SWITCHED-CARRIER TRANSCIEVER**

(75) Inventors: Kurt Holmquist, Largo, FL (US);  
 Joseph Chapman, Seminole, FL (US)

(73) Assignee: Paradyne Corporation, Largo, FL (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 812 days.

(21) Appl. No.: 09/637,185

(22) Filed: Aug. 11, 2000

#### Related U.S. Application Data

(60) Provisional application No. 60/150,436, filed on Aug. 24, 1999.

(51) Int. Cl.<sup>7</sup> ..... H04L 12/56

(52) U.S. Cl. .... 370/476; 370/477

(58) Field of Search ..... 370/476, 471, 370/472, 474, 477, 389

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 6,651,210 B1 \* 11/2003 Troll et al. .... 714/758

\* cited by examiner

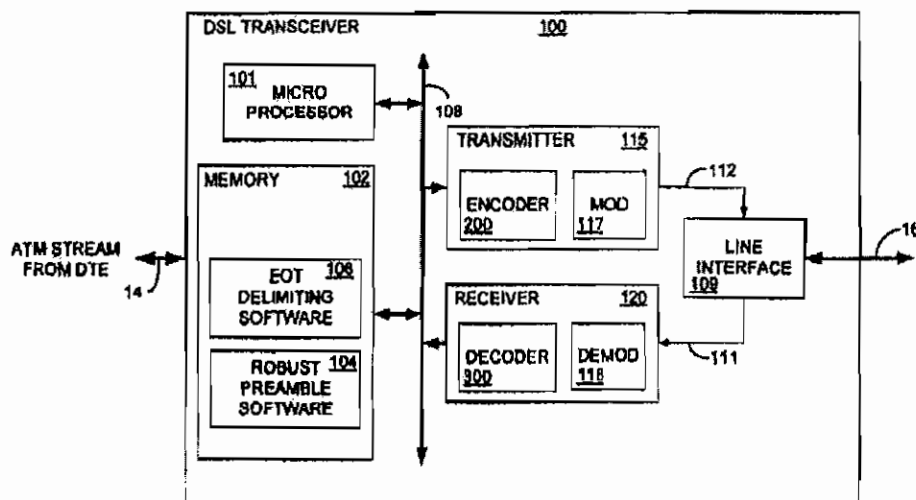
Primary Examiner—Kenneth Vanderpuye

(74) Attorney, Agent, or Firm—Thomas, Kayden, Horstemeier & Risley LLP

#### (57) ABSTRACT

A method and system for robust delimiting of transmitted messages in switched-carrier operation in which a preamble precedes each communication message with the preamble comprising symbols transmitted at a rate lower than that of the following data. The lower rate symbols of the preamble significantly increase the probability that the decoder will decode the preamble symbols error free. Communication line control information can be included in the robust preamble, thereby ensuring that line control information is reliably transferred over the communication channel. The first symbol of the preamble can be transmitted at the lower symbol rate and at an increased power level, thereby clearly and reliably delimiting the beginning of a transmission. The end of the communication message can be reliably delimited by sending the first symbol containing only bits from a next cell of information at a lower symbol rate and including an extra bit in that symbol. The extra bit can be set to indicate to a receiver whether the last cell of information has just begun.

55 Claims, 10 Drawing Sheets

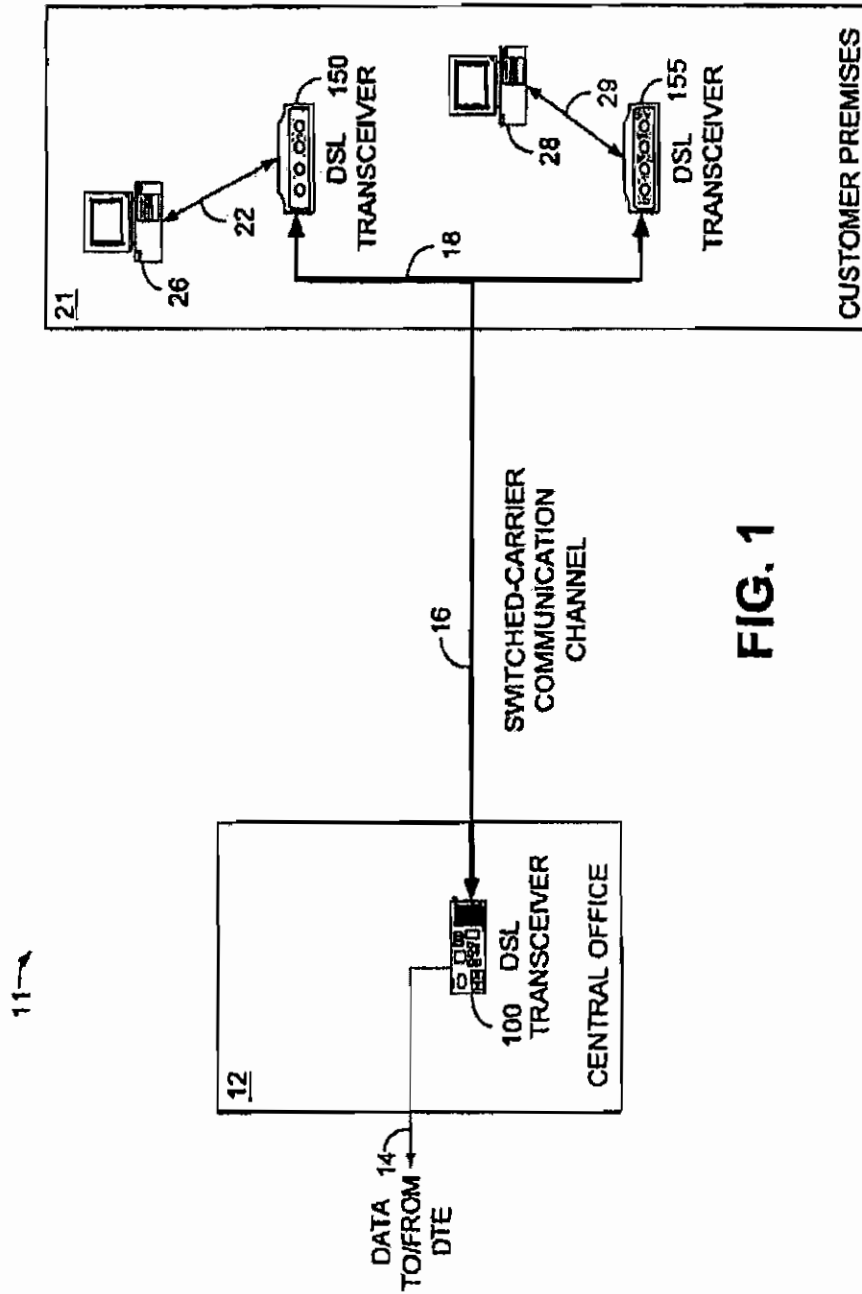


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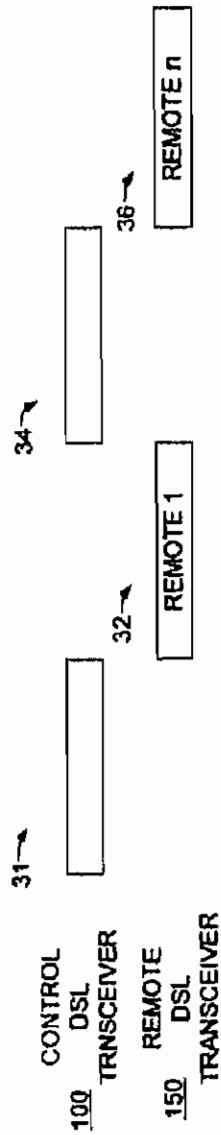


FIG. 2A

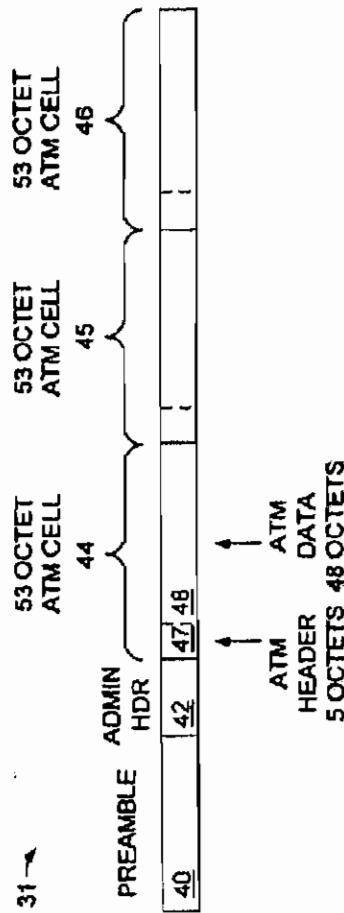
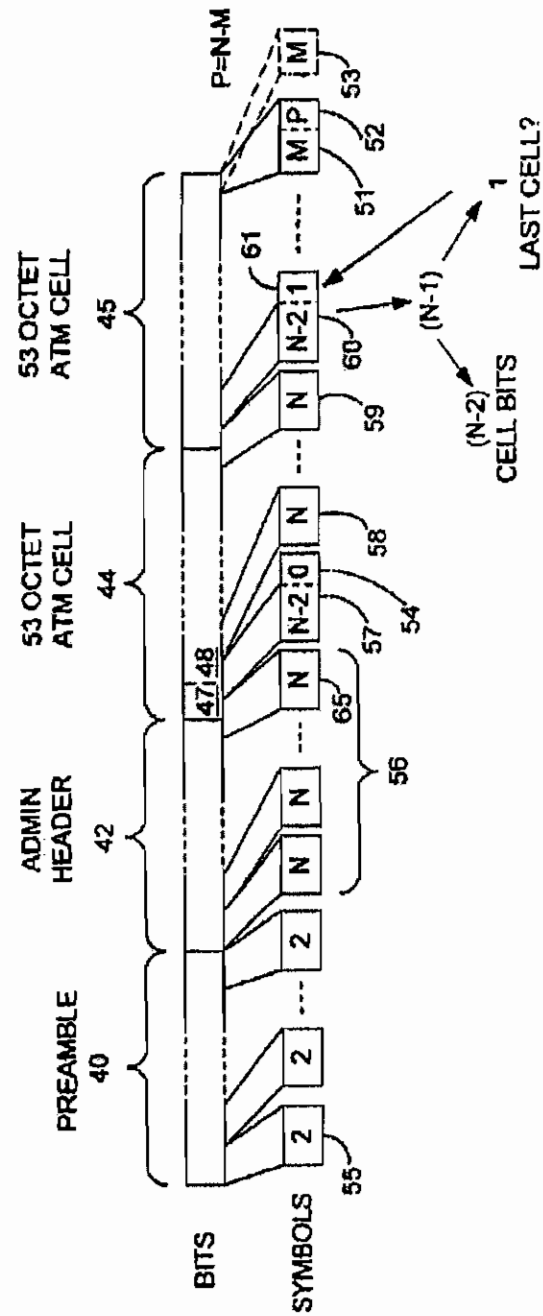


FIG. 2B

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**FIG. 3A**

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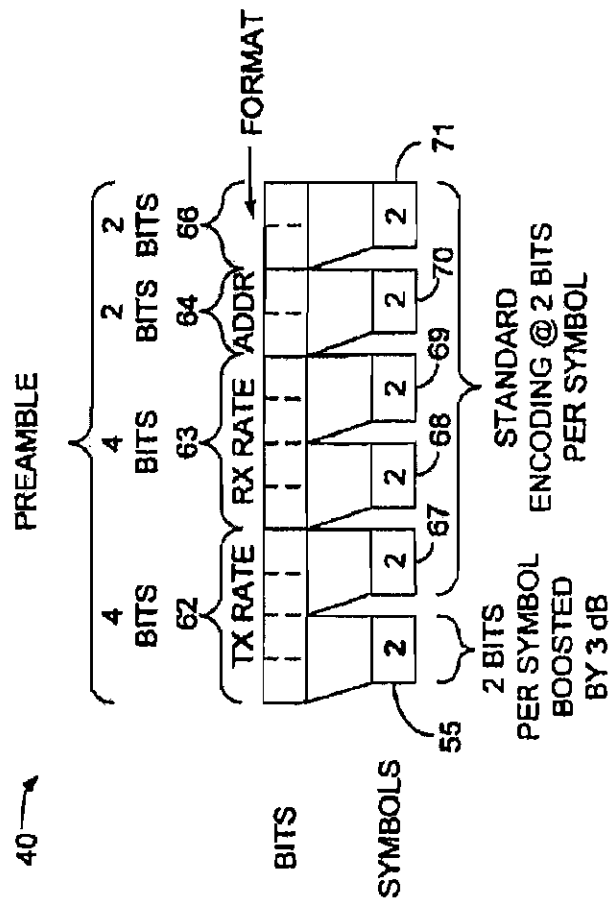


FIG. 3B

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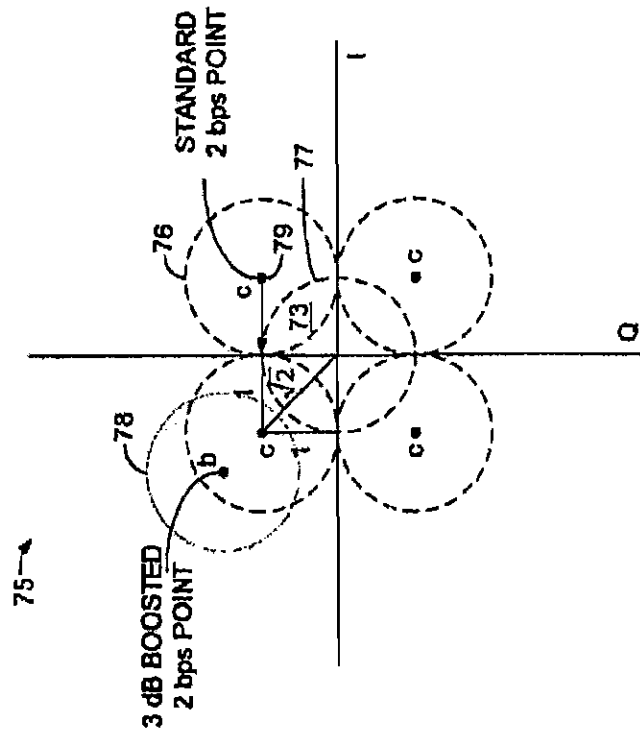


FIG. 4A

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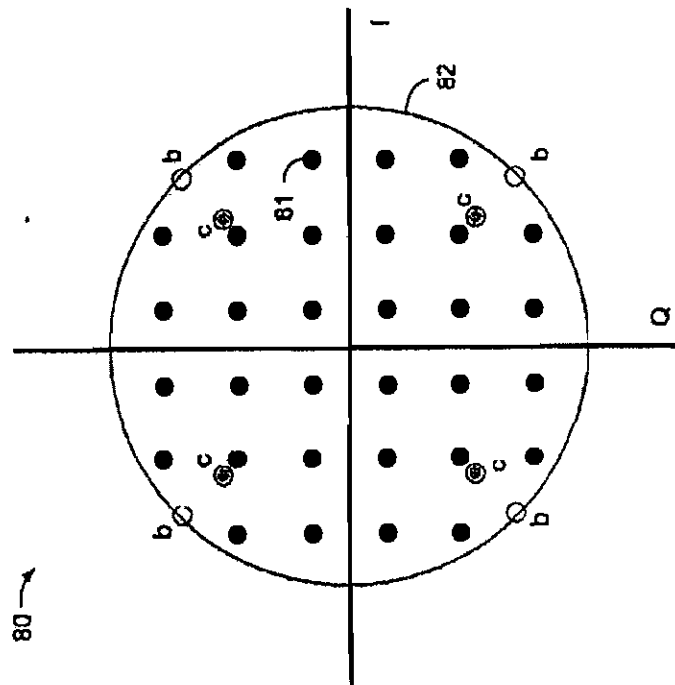
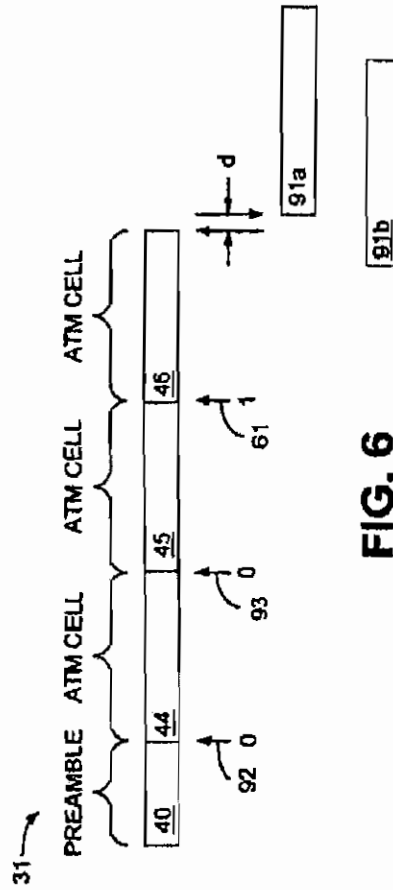
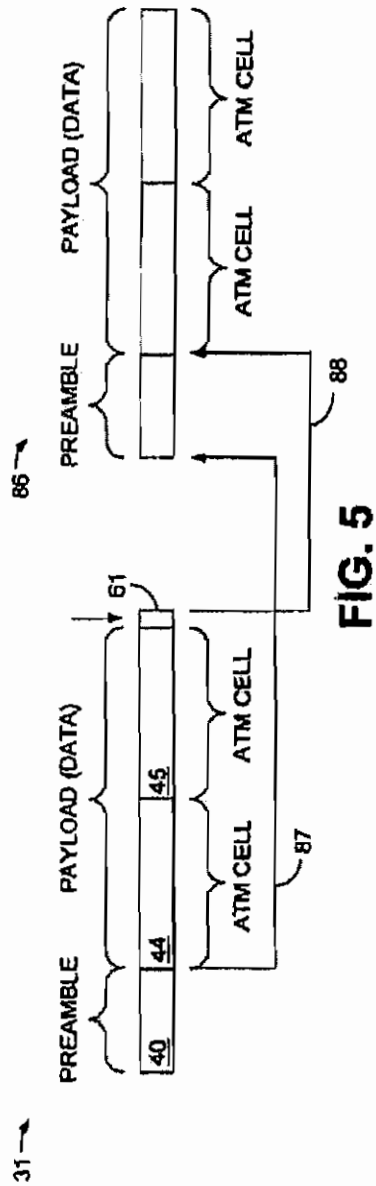


FIG. 4B



U.S. Patent

Sep. 27, 2005

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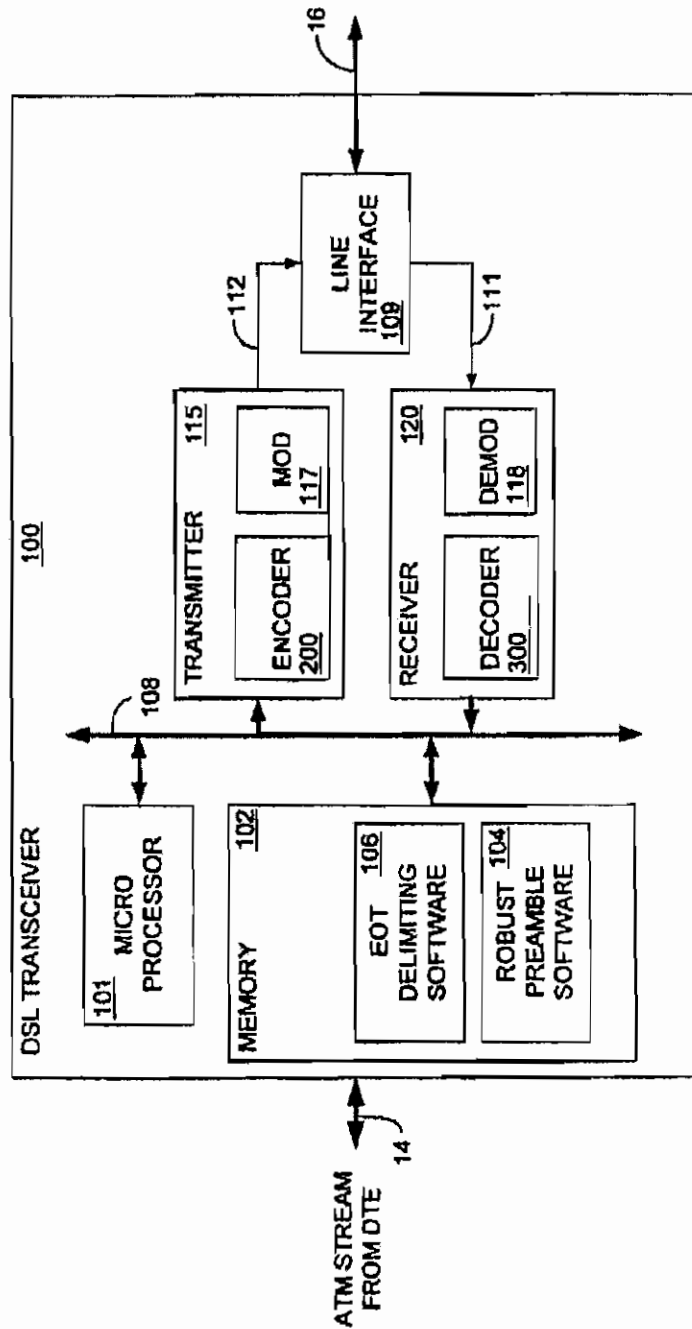
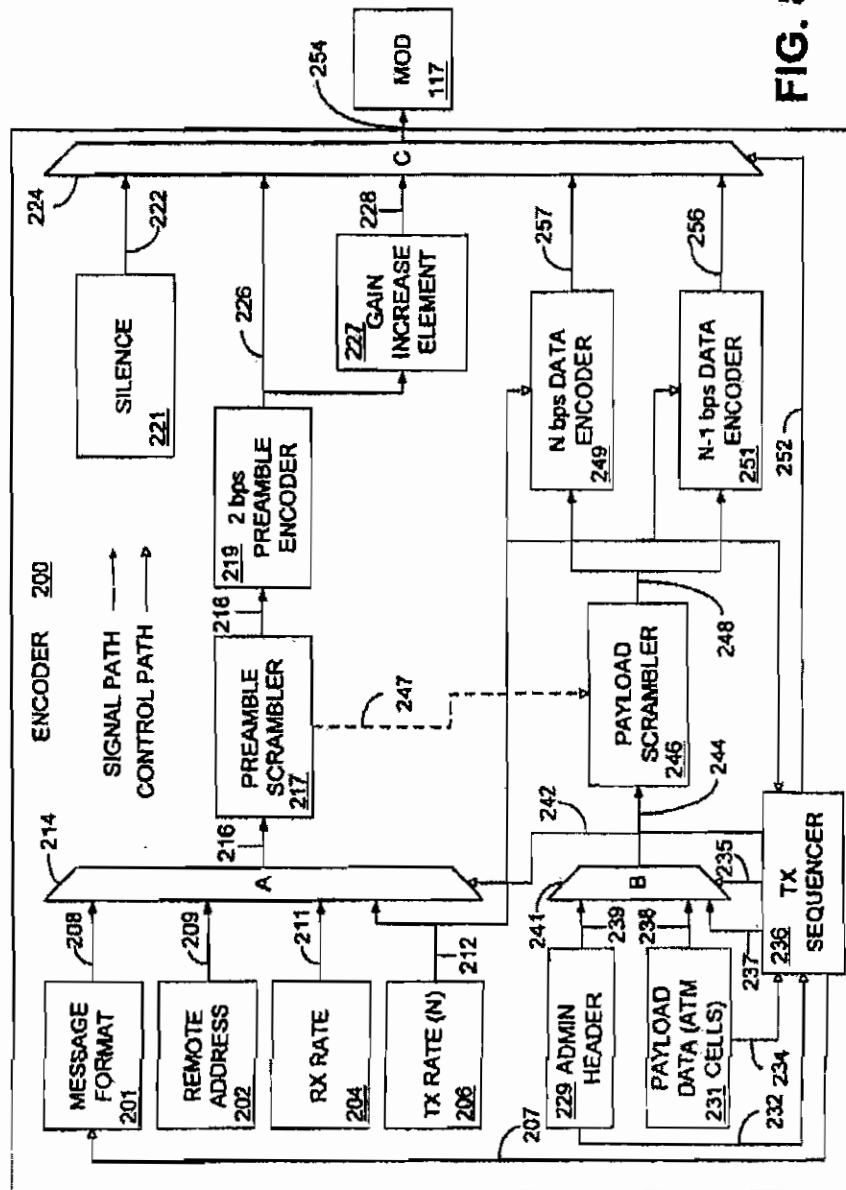


FIG. 7



**FIG. 8**

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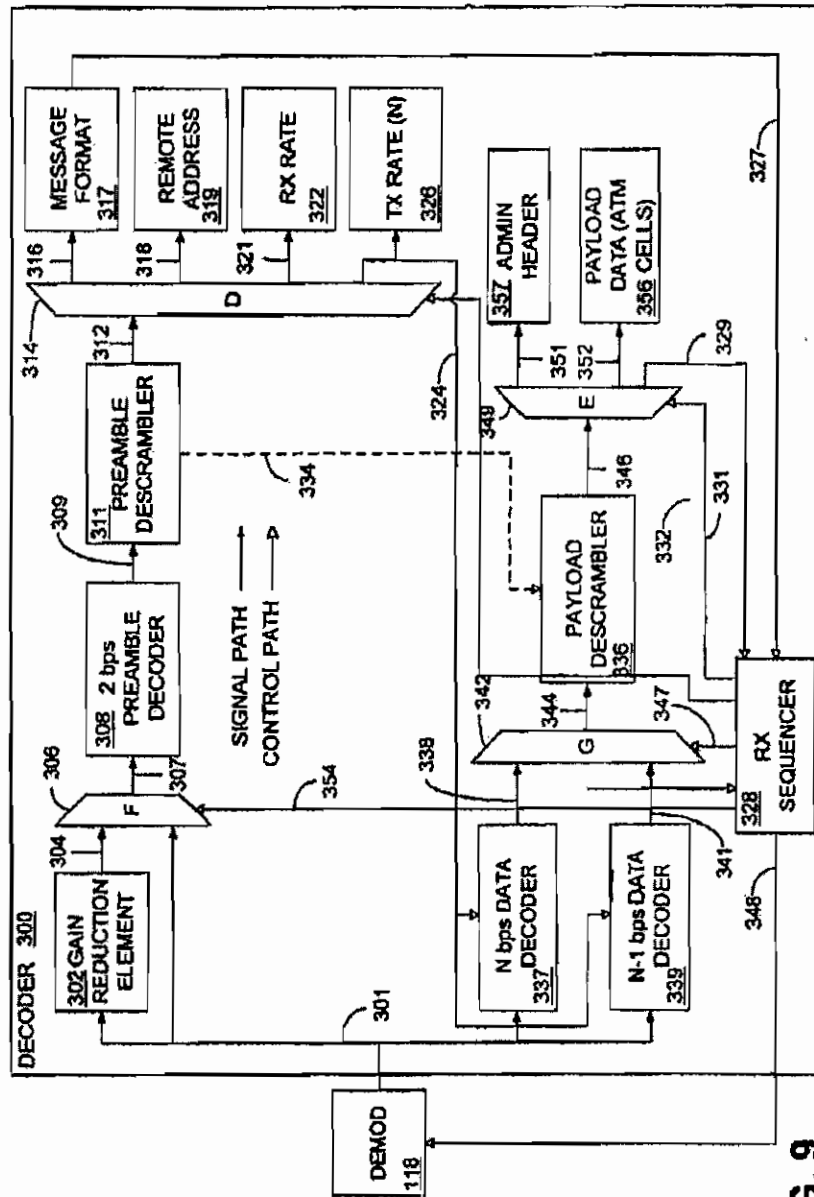


FIG. 9

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# SYSTEM AND METHOD FOR A ROBUST PREAMBLE AND TRANSMISSION DELIMITING IN A SWITCHED-CARRIER TRANSCIVER

## CROSS-REFERENCE TO RELATED APPLICATIONS

This document claims priority to, and the benefit of, the filing date of Provisional Application Ser. No. 60/150,436 entitled "A TECHNIQUE FOR ROBUST SIGNAL DELIMITING AND ENCODING OF CRITICAL LINK CONTROL SIGNALS APPLIED TO TRANSMISSION OF ATM CELLS OVER A DSL USING ADAPTIVE TIME DOMAIN DUPLEX (ATDD)," filed on Aug. 24, 1999, which is hereby incorporated by reference.

## TECHNICAL FIELD

The present invention relates generally to communication systems, and more particularly, to a system and method for a robust preamble and transmission delimiting in a switched-carrier transceiver.

## BACKGROUND OF THE INVENTION

Data communication typically occurs as the transfer of information from one communication device to another. This is typically accomplished by the use of a modem located at each communication endpoint. In the past, the term modem denoted a piece of communication apparatus that performed a modulation and demodulation function, hence the term "modem". Today, the term modem is typically used to denote any piece of communication apparatus that enables the transfer of data and voice information from one location to another. For example, modem communication systems use many different technologies to perform the transfer of information from one location to another. Digital subscriber line (DSL) technology is one vehicle for such transfer of information. DSL technology uses the widely available subscriber loop, the copper wire pair that extends from a telephone company central office to a residential location, over which communication services, including the exchange of voice and data, may be provided. DSL devices can be referred to as modems, or, more accurately, transceivers, which connect the telephone company central office to the user, or remote location typically, referred to as the customer premises. DSL communication devices utilize different types of modulation schemes and achieve widely varying communication rates. However, even the slowest DSL communications devices achieve data rates far in excess of conventional point-to-point modems.

DSL transceivers can be used to provision a variety of communication services using, for example, asynchronous transfer mode (ATM). ATM defines a communication protocol in which 53 octet (byte) cells are used to carry information over the DSL communication channel. The first five octets of the ATM cell are typically used for overhead and the remaining 48 octets are used to carry payload data. When using a switched-carrier transmission methodology, a control transceiver may be connected via the DSL to one or more remote transceivers. In such a communication scheme, the transmission is commonly referred to as a "half-duplex," which is defined as two way electronic communication that takes place in only one direction at a time. With only a single remote transceiver on a line, switched-carrier transmission may instead be employed in full-duplex mode (i.e., allowing transmission in both directions simultaneously). In this case, full-duplex operation is typically enabled by employing

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either echo cancellation or frequency division multiplexing. Hybrid techniques are possible such as one in which there are multiple remote transceivers and communication takes place between the control transceiver and only one remote transceiver in full-duplex fashion. As it relates to the present invention, the common characteristic of these communication techniques is the use of a switched-carrier modulation in which transmitters are deliberately silent for some interval between signal transmissions. For simplicity, the following discussions assume the simplest case of using switch carrier modulation with a half-duplex (also sometimes referred to as "time domain duplex") line usage discipline.

Before the transmission of ATM cells, a preamble containing channel, transmission, address and administrative information may be transmitted by the transceiver. The application of this preamble is sometimes referred to as "framing" the data to be transmitted. Due to the switched-carrier nature of the transmission, silence precedes this preamble and it is of course important for all symbols in this preamble to be received error free. It is also desirable to have the ability to precisely delimit the beginning and end of a transmission to within one transmitted symbol interval. Robustly delimiting the beginning of a message enables a receiving transceiver to reliably begin immediately decoding the message at the correct symbol. Likewise, robustly delimiting the end of a message enables a receiving transceiver to reliably decode the entire message through the final symbol and then stopping so as to prevent data loss and to prevent the inclusion of any false data. Furthermore, by communicating the end of message indicator to a receiving transceiver prior to the actual end of the message, line turnaround time (i.e., idle time on the line between transmissions) can be reduced, thereby increasing the effective use of the available line bandwidth.

Because the most efficient signal constellation encoding cannot allocate signal space to silence, it is impractical to reliably discriminate silence from a signal when analyzing only a single symbol encoding an arbitrary data value.

To improve message delimiting, existing techniques use special marker symbols whose symbol indices are greater than those used to encode data. At N bits per symbol (bps) data is encoded using symbol indices 0 through  $2^N - 1$ . The special marker symbols use indices  $2^N$  and above. While these special marker symbols are useful for marking the beginning and end of a transmission, their placement at the outer edges of a constellation raises the peak signal, thus increasing the peak to average ratio (PAR) across all data rates by as much as 4 dB. Unfortunately, discrimination of special symbols has the same error threshold as does decoding of data.

Thus, it would be desirable to have a robust manner in which to detect the beginning and end of a transmission so that line bandwidth can be most efficiently allocated. Furthermore, it would be desirable to robustly transmit a message preamble including control information thereby greatly improving the probability that the preamble is received error free.

## SUMMARY OF THE INVENTION

The present invention provides an improved system and method for robustly delimiting a message transmission in switched-carrier communication systems. The invention provides a method and system for transmission of a message preamble in which transmission of the preamble is more robust than the data. In this manner, the beginning and end of a transmission can be robustly delimited and channel control information can be reliably conveyed to a receiving transceiver.

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The system of the present invention uses a novel header application, which enables the transport of ATM, or any other data, efficiently and economically over a communications channel, such as a DSL communications channel.

Briefly described, in architecture, the system for robust transmission delimiting comprises a communication message including a preamble including a plurality of bits representing communication link control information, and an encoder configured to encode the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel.

In another aspect, the invention is a system for delimiting the end of a transmission. The system takes a communication message segmented into a plurality of fixed size units, each fixed size unit including a plurality of bits, and includes an encoder configured to encode the plurality of bits into a plurality of symbol indices at a first data rate. The encoder is also configured to encode the first symbol index containing only bits from each fixed size unit at a data rate lower than that of the first data rate.

The present invention can also be viewed as a method for robust transmission delimiting comprising the steps of applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information, and encoding the preamble bits into a plurality of symbol indices. The symbol indices are encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

In another aspect, the invention is a method for delimiting the end of a transmission comprising the steps of segmenting a communication message into a plurality of fixed size units, each unit including a plurality of bits, encoding a plurality of the bits in the units into a plurality of symbol indices, the symbol indices being encoded at a first rate, and encoding the first symbol index containing only bits from each fixed size unit at a rate lower than that of the first rate.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The invention can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present invention. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

FIG. 1 is a schematic view illustrating a switched-carrier half-duplex communication environment, in which DSL transceivers containing the present invention reside;

FIG. 2A is an illustration of the time-domain duplex communication methodology employed by the DSL transceivers of FIG. 1;

FIG. 2B is a schematic view illustrating, in further detail, a communication message of FIG. 2A;

FIG. 3A is a schematic view illustrating the bit to symbol relationship of the communication message of FIG. 2B;

FIG. 3B is a schematic view illustrating, in further detail, the preamble of FIG. 3A;

FIG. 4A is a graphical illustration representing a two (2) bit per symbol signal space constellation and the increased energy symbol of FIG. 3B;

FIG. 4B is a graphical illustration showing an exemplar grouping of constellation points representing different bit per symbol rates in accordance with an aspect of the invention;

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FIG. 5 is a schematic view illustrating the communication message of FIG. 3A and a technique for scrambling that further improves reliable transmission of the message preamble;

FIG. 6 is a schematic view illustrating the communication message of FIG. 3A and the reduced line turn around delay made possible by an aspect of the invention;

FIG. 7 is a block diagram illustrating the control DSL transceiver of FIG. 1;

FIG. 8 is a block diagram illustrating the encoder of FIG. 7; and

FIG. 9 is a block diagram illustrating the decoder of FIG. 7.

#### DETAILED DESCRIPTION OF THE INVENTION

Although, described with particular reference to the transmission of ATM cells over a DSL communication channel, the system and method for a robust preamble and transmission delimiting can be implemented to transmit all forms of data in any switched-carrier transmission system in which it is desirable to send a robust preamble and to robustly delimit the beginning and end of each communication message.

Furthermore, the system and method for a robust preamble and transmission delimiting can be implemented in software, hardware, or a combination thereof. In a preferred embodiment(s), selected portions of the system and method for a robust preamble and transmission delimiting are implemented in hardware and software. The hardware portion of the invention can be implemented using specialized hardware logic. The software portion can be stored in a memory and be executed by a suitable instruction execution system (microprocessor). The hardware implementation of the system and method for a robust preamble and transmission delimiting can include any or a combination of the following technologies, which are all well known in the art: a discrete logic circuit(s) having logic gates for implementing logic functions upon data signals, an application specific integrated circuit having appropriate logic gates, a programmable gate array(s) (PGA), a field programmable gate array (FPGA), etc.

Furthermore, the robust preamble and transmission delimiting software, which comprises an ordered listing of executable instructions for implementing logical functions, can be embodied in any computer-readable medium. Moreover, use by or in connection with an instruction execution system, apparatus, or device, such as a computer-based system, processor-containing system, or other system that can fetch the instructions from the instruction execution system, apparatus, or device and execute the instructions.

In the context of this document, a "computer-readable medium" can be any means that can contain, store, communicate, propagate, or transport the program for use by or in connection with the instruction execution system, apparatus, or device. The computer readable medium can be, for example but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, device, or propagation medium. More specific examples (a non-exhaustive list) of the computer-readable medium would include the following: a electrical connection (electronic) having one or more wires, a portable computer diskette (magnetic), a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory) (magnetic), an optical fiber (optical), and a portable compact disc read-only memory (CDROM) (optical). Note that the computer-

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readable medium could even be paper or another suitable medium upon which the program is printed. As the program can be electronically captured, via for instance optical scanning of the paper or other medium, then compiled, interpreted or otherwise processed in a suitable manner if necessary, and then stored in a computer memory.

Turning now to the drawings, FIG. 1 is a schematic view illustrating a switched-carrier half-duplex communication environment 1, in which DSL transceivers containing the present invention reside. Although the invention will be described below in a half-duplex communication environment, the DSL transceivers containing the invention may be used in a switched-carrier full-duplex environment as well. In such a case, full-duplex operation may be enabled using technologies such as echo cancellation or frequency division multiplexing. Communication environment 1, includes central office 12 connected via communication channel 16 to customer premises 21. Communication channel 16 can be any physical medium over which communications signals can be exchanged, and in the preferred embodiment, is the copper wire pair that extends from a telephone company central office to an end-user location, such as a home or office. Central office 12 includes DSL transceiver 100 connected to communication channel 16. DSL transceiver 100 processes data via connection 14. DSL transceiver 100 exchanges data via connection 14 with any data terminal equipment (DTE), such as a computer or data terminal.

Customer premises 21 includes one or more DSL transceivers 150 connected via internal infrastructure wiring 18 to communication channel 16. The infrastructure wiring 18 can be, for example but not limited to, the telephone wiring within a private residence or within an office. DSL transceivers 150 can be connected to a variety of telecommunication devices located at customer premises 21. For example, DSL transceiver 150 connects via connection 22 to a personal computer 26. Although additional DSL transceivers can be located at customer premises 21, an exemplar one of which is indicated using reference numeral 155, the aspects of the invention to be discussed below are also applicable if only one DSL transceiver 150 is located at customer premises 21. In the example given in FIG. 1, DSL transceiver 155 connects to computer 28 via connection 29.

The DSL transceiver 100 located at central office 12 is considered a "control device" and the DSL transceiver 150 located at customer premises 21 is considered a "remote device." This is so because the control DSL transceiver 100 controls the communication sessions by periodically polling each remote DSL transceiver 150 to determine whether the remote device has information to transmit. Regardless of the number of DSL transceivers located at customer premises 21, the method of communication between DSL transceiver 100 located at central office 12 and DSL transceiver 150 located at customer premises 21 is half-duplex in nature, sometimes referred to as adaptive time-domain duplex, or data driven half-duplex, unless the above-mentioned technologies such as echo cancellation or frequency division multiplexing allow full-duplex operation between the control transceiver 100 and one remote transceiver 150. This means that during any time period only one DSL transceiver may transmit at any time. In the situation in which there are multiple DSL transceivers located at customer premises 21, the DSL transceiver 100 located at central office 12 periodically polls each DSL transceiver located at customer premises 21 at an appropriate time to determine whether any of the remotely located DSL transceivers have any information to transmit to central office 12. If only one DSL

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transceiver 150 is located at customer premises 21, the communication method may be half-duplex in nature or conventional full-duplex techniques may be used (e.g., using either frequency division multiplexing or echo cancellation).

FIG. 2A is a schematic view illustrating the time-domain duplex communication methodology between a control DSL transceiver 100 and a remote DSL transceiver 150. When a control DSL transceiver 100 desires to send a message to a remote DSL transceiver 150 (the control DSL transceiver 100 sends a communication message 31 including a preamble and any information that is to be transmitted. There are times when the communication message may include only a preamble. After the transmission of communication message 31, the remote DSL transceiver to which communication message 31 is addressed (in this example remote DSL transceiver 150) responds with communication message 32. After the remote DSL transceiver 150 completes the transmission of communication message 32, the control DSL transceiver 100 is now free to send another communication message 34 to either the same remote DSL transceiver 150 or, if present, a different remote DSL transceiver, such as DSL transceiver 155 (remote "n") of FIG. 1. As illustrated in FIG. 2A, remote DSL transceiver "n" responds with communication message 36. In this manner, the communication methodology between control DSL transceiver 100 and all remote DSL transceivers 150, 155 . . . n, is switched-carrier and time-domain duplexed.

FIG. 2B is a schematic view illustrating, in further detail, the communication message 31 of FIG. 2A. Communication message 31 begins with preamble 40 followed by optional administrative header 42. In accordance with an aspect of the invention, all communication messages, regardless of the content, begin with preamble 40. Administrative header 42 is optional and can be used to send information that is neither part of the preamble 40 or of any data to follow. For example, the administrative header 42 could convey a description of noise level conditions at one end so the other end may opt to increase or reduce the power level of its transmission as necessary. Likewise, the administrative header 42 sent by a remote transceiver could contain information regarding the amount of payload information that the remote transceiver is ready to transmit and its relative priorities so that the control transceiver could alter the amount of time that this remote transceiver is given to transmit its data (relative to any other transceivers connected to the line). When the payload data comprises ATM cells, the control transceiver could use messages conveyed by the administrative header 42 to direct remote devices to activate or deactivate various ATM virtual circuits.

If data is included in communication message 31, one or more ATM cells follow the optional administrative header 42. Although illustrated using three ATM cells, 44, 45 and 46, there are situations in which no ATM cells, or for that matter, no information of any kind, follows preamble 40. In the case in which information does follow preamble 40, and for purposes of illustration only, ATM cells 44, 45 and 46 are each standard 53 octet ATM cells. For example, ATM cell 44 includes 5 octet ATM header 47 and 48 octets of ATM data 48. ATM cells 45 and 46 are identical in structure to ATM cell 44. ATM cells 44, 45 and 46 adhere to the conventional ATM cell structure as defined in standardized ATM literature. It should be noted that optional administrative header 42 does not follow the standard ATM cell format and that administrative header 42 can be any number of octets in length. As known to those having ordinary skill in the art, an octet comprises 8 bits of information. Although described with particular reference to the transportation of ATM cells

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over a DSL communication channel), the principles of the invention are applicable to all fixed length communication messages.

FIG. 3A is a schematic view illustrating the bit to symbol relationship of the communication message 31 of FIG. 2B. In accordance with an aspect of the invention, preamble 40 is placed at the beginning of every transmission (i.e., each communication message 31). Preamble 40 is followed by optional administrative header 42, which is then followed, if there is data to transmit, by one or more 53 octet ATM cell 44 and 45. Although illustrated using only two ATM cells, any number of ATM cells may follow preamble 40 and, if included, optional administrative header 42. The ATM cells are a stream of data information represented as a series of bits that are placed into each ATM cell.

The preamble 40 is also a series of bits, which are encoded into a number of communication symbols. Symbols are the representation of the bits to be transmitted, and are represented as signal points in a signal space constellation (to be described below with respect to FIGS. 4A and 4B). In accordance with one aspect of the invention, each of the bits in preamble 40 are encoded into symbols, an exemplar one of which is illustrated using reference numeral 55, at the lowest available bit rate that can be transmitted over the communication channel 16. For purposes of illustration only, the symbols that encode the bits in the preamble 40 shown in FIG. 3A are encoded at a rate of two (2) bits per symbol. However, any number of bits per symbol lower than that of the normally transmitted data rate can be used so long as the symbol rate allows a receiving device to more reliably decode those symbols. For example, if the normal data rate is five (5) bits per symbol, then a symbol rate of two (2) bits per symbol has a significantly (approximately 9 dB) higher noise margin than the five (5) bit per symbol data rate, thereby allowing the symbols that are encoded at the lower rate of two (2) bits per symbol to be very robustly and reliably decoded by a receiving device. In this manner, the preamble 40, which is sent at the beginning of every communication message 31, can be made sufficiently robust so that the chance that it will always be received error free is greatly increased. Although very robust, there are still situations in which the symbols into which the preamble bits are encoded can be corrupted. However, in accordance with another aspect of the invention, because the preamble 40 is sent at the beginning of every communication message 31, even if the preamble 40 is corrupted, only data following that preamble may be affected, i.e., lost due to corruption, if certain bits of the preamble are corrupted.

In accordance with another aspect of the invention, the first symbol 55 representing the first bits in the preamble 40 can be sent using an increased power level, thereby clearly and robustly delimiting the beginning of the communication message 31. The effect of this increased power level symbol 55 will be explained in greater detail below with respect to FIGS. 4A and 4B.

Still referring to FIG. 3A, if an administrative header 42 is present in communication message 31, then the bits that are contained to administrative header 42 will be encoded at a symbol rate of "N" bits per symbol, where N is the normal data rate. The normal data rate can be any data rate, for example, but not limited to, a value between 2 and 12 (inclusive) bits per symbol. For purposes of illustration, and for simplicity of explanation, the normal symbol rate can be five bits per symbol. This is represented by the group of symbols 56 into which all the bits of administrative header 42 and a portion of the bits of header 47 of ATM cell 44 are encoded.

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In accordance with another aspect of the invention, the first symbol used to encode bits from a particular cell that contains bits only from that cell will be encoded at a data rate lower than that of the standard data rate used for all other bits of each cell. For example, symbol 57 is the first symbol that contains bits only from ATM cell 44. The last symbol 65 of symbol group 56 contains bits from both administrative header 42 and ATM cell 44. Likewise, symbol 60 is the first symbol containing only bits from ATM cell 45. In accordance with this aspect of the invention, the symbols 57 and 60 will be encoded at a data rate that is two (2) bits per symbol lower than that of the preceding symbol (represented by N-2 where N is the number of bits per symbol used for encoding all other bits of the administrative header and ATM cells.) In this manner, because of the fixed length 53 octet ATM cells, by simple bit counting, the receiver will always know the first symbol encoding bits from a cell that contains only bits from this cell, and therefore has the special encoding described herein. These N-2 bits of the cell data are grouped for transmission and an additional bit (bit 54 of cell 44 or bit 61 for cell 45) is added for a total of N-1 bits encoded into symbol 57 or 60, respectively. This group of N-1 bits, represented by symbol 57 or 60, is encoded into a symbol and scaled for transmission with the scaling normally applied when encoding at N-1 bits per symbol. The extra bit 54 or 61 indicates whether or not the cell just started (ATM cell 44 or 45, respectively) is the last cell of the transmission. The extra bit 61 in symbol 60 is set to logic one to indicate that ATM cell 45 is the last cell of the transmission so that the receiver will know at the beginning of the receipt of ATM cell 45 that ATM cell 45 is the last cell in the transmission. For the same reason, bit 54 in symbol 57 set to zero so that the receiver will know that at least one more cell follows cell 44.

If N=2, then no bits are taken from the cell to encode the next symbol (since N-2=0). Since N-1=1, the next symbol contains just one bit, which is the last cell indicator. This effectively inserts an entire extra symbol in each cell. Nevertheless, the same encoding/decoding logic for this special symbol applies for any value of N $\geq$ 2.

Once the receiver knows that a particular cell is the last cell in the message, by simple counting it can readily identify the symbol that contains the last bits of the last cell. This is represented in FIG. 3A as symbol 51 or optionally symbol 53. Since the number of bits remaining to be transmitted in the last symbol (M) can be less than N, a modified encoding technique is preferable for this symbol. One option is to add one or more padding bits (P) 52 so that M+P=N. Another option is to encode the last group of bits at M bits per symbol as represented by symbol 53. This has the advantage of increased robustness for the transmission of these bits.

For simplicity, the following discussion does not address this second technique. Having recognized the last symbol of the transmission, the receiver does not attempt to demodulate and decode the signal on the line following this symbol since the transmitting station must now be sending silence.

It should be noted that although described as being encoded at N-1 bits per symbol, the symbols 57 and 60 containing the additional last cell indicator bit can be encoded at any symbol rate lower than that of the standard transmission rate (N bits per symbol). For example, if N is five (5), the specially encoded symbols could also be encoded at N-2 or three (3) bits per symbol so that they contain two (2) bits of cell data plus the last cell indicator bit. In this manner, the receiver can clearly and reliably decode the symbol 60, thereby providing a robust and reliable end of message delimiter.

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In accordance with this aspect of the invention, and to be described in further detail with respect to FIG. 3B, it is also desirable to have the ability to indicate that a message contains only an administrative header 42. In order to accomplish this, the first symbol containing data from the administrative header 42 can also be encoded using the higher noise margin N-1 bit per symbol encoding technique described above. For example, the first N-2 bits of the administrative header 42 can be combined with a last cell bit (such as bit 61 of symbol 60) and be encoded at the N-1 bit per symbol rate. This can provide the extra bit to indicate whether or not one or more ATM cells follow administrative header 42. An alternative technique is to simply include a bit in the preamble 40 that indicates whether an administrative header 40 follows the preamble. For simplicity, it has been assumed that this alternative technique is used with respect to FIG. 3A and in the following discussion.

Because each ATM cell is the smallest unit of a payload of ATM cells, and because all ATM cells have the same length, the first symbol of each cell that carries only bits of that cell can readily be identified. Because these bits are transmitted using the specially encoded symbol carrying two fewer bits than normal (as described above), the length of each cell is effectively increased by two bits. In some cases this can result in one extra symbol being needed to transmit the cell. In other cases an additional cell is not needed because the spare bits are available anyway (and would have ended up as the padding bits (P) 52 in FIG. 3A). Because the cells may be transmitted contiguously as a bit stream, the addition of one extra symbol may provide sufficient extra bits to cover the opening symbol of multiple following cells. For example, at eight (8) bits per symbol, in one (1) extra symbol is needed to cover the end of frame signaling overhead to transmit up to four (4) cells.

FIG. 3B is a schematic view illustrating, in further detail, the exemplar preamble 40 of FIG. 3A. The bit stream of preamble 40 comprises four (4) bits 62 that include information regarding the transmit rate (in bits per symbol) used to encode data following preamble 40 (the data comprising the optional administrative header and optional ATM cells), four (4) bits 63 that include information regarding the rate (also in bits per symbol) that the receiver is capable of receiving, two (2) bits 64 that identify the address of a remote DSL transceiver if the control DSL transceiver is transmitting (if a remote DSL transceiver is transmitting, then these two (2) bits 64 can represent the address of that remote DSL transceiver) and two (2) bits 66, which can be used to communicate the format of the message to follow. For example, the two (2) bits 66 can be used to advise a receiving device whether an administrative header 42 follows the preamble 40, whether ATM cells follow the preamble, whether both follow or whether only the preamble is being transmitted. The four (4) bits provided by symbols 55 and 67 and by symbols 68 and 69 can each encode as many as sixteen data encoding rates.

As mentioned above, the preamble 40 is sent at the beginning of each transmission. The twelve (12) bits that comprise the preamble 40 are encoded into symbols 55, 67, 68, 69, 70 and 71 in accordance with that described above. In accordance with an aspect of the invention, all of the symbols in preamble 40 are encoded at a low bit per symbol rate. In this example, all of the symbols are encoded at a rate of two (2) bits per symbol, however, any other low bit per symbol rate can be used with similar results. The low bit per symbol rate ensures a high signal-to-noise ratio for these symbols, thereby significantly decreasing the probability that these preamble symbols will be corrupted by noise on

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the communication channel. The payload data (administrative header and ATM cells) would typically be encoded at N bits per symbol only if transmission at this N bit per symbol rate has an acceptably low rate of errors (based on line length, signal strength, noise, distortion and other impairments that may be present). Otherwise, data transmission efficiency would suffer. Therefore, encoding the preamble at less than N bits per symbol allows a corresponding improvement in the reliability of transmitting this information such that it is highly unlikely to be corrupted. Since very few bits are needed to convey the information carried in the preamble, a very low rate can be used without seriously reducing the overall transmission efficiency.

In accordance with another aspect of the invention, the first symbol 55 is encoded at a rate of two (2) bits per symbol and has its energy increased to a point at which noise on the communication channel is unlikely to cause a receiver to erroneously interpret the first symbol 55 as silence. Likewise the increased energy makes it unlikely that noise on the communication channel will cause the receiver to erroneously interpret an interval of the silence that precedes each message as the starting symbol of a message. It has been found that an energy increase of 3dB is sufficient. This aspect of the invention will be described in greater detail below with respect to FIGS. 4A and 4B. In this manner, the beginning of each transmission can be clearly and robustly delimited. The remainder of the symbols 67, 68, 69, 70 and 71 that represent the bits in preamble 40 are all encoded at two (2) bits per symbol, but do not have their energy increased.

The four (4) transmit rate bits 62 inform a receiving DSL transceiver of the transmit rate of the information to follow the preamble 40. Sending this information in every message has significant benefits. It provides the transmitting transceiver the option of changing the encoding rate for the payload from one message to the next. Messages containing information that has been determined to be of high priority can be transmitted using a lower number of bits per symbol to improve the chances of its being received without errors. If the communications system intermittently has a reduced throughput demand, the transceivers may instantly reduce their data rates to improve robustness without adversely affecting real throughput. Finally, if a severe noise condition (such as an impulse caused by plain old telephone service (POTS) ringing signals on a subscriber line 16) happens to corrupt one or both of the symbols 55 and 67 that encode the transmit rate, only the payload data in this message will be improperly decoded. The receiver's memory of a corrupted rate value lasts only until the next transmission begins. This allows the transmit rate to potentially be changed for every message while at the same time avoiding the complexities of providing fail-safe communication of the rate, such as through use of an automatic repeat request (ARQ) protocol, that would be needed if the rate is sent only when it is changed.

The receive rate bits 63 allow the transmitting device to communicate to the receiving device the maximum receive rate at which the transmitting device can receive. Information included in these receive rate bits 63 are commands that instruct the opposite device to either increase or decrease its transmit rate. This allows the responding transceiver to instantly modify the rate it uses for its next transmission to accommodate changes in the signal quality that have been detected at the opposite end of the line.

In accordance with an aspect of the invention, the address bits 64 need only be used when the control DSL transceiver

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100 is communicating with a plurality of remote DSL transceivers in what is commonly referred to as "multi-point" mode. When communicating in "multi-point" mode the address bits 64 include either the address of the remote DSL transceiver 150 that is to transmit next (if the transmission is sent by the control DSL transceiver 100) or the address of the responding remote DSL transceiver 150 (if the transmission is sent by the remote DSL transceiver 150). Sending these bits 64 at the lower bit rate of the preamble reduces the likelihood of a remote transceiver 150 not responding or of the incorrect remote transceiver 150 responding to a message from the control transceiver 100. Frequent occurrences of either of these two types of errors could adversely affect the overall data transmission efficiency of the line.

The format bits 66 indicate whether the optional administrative header 42 is being sent, whether one or more ATM cells are being sent, or whether both or neither are being sent. As described previously, the receiver uses this information in conjunction with the transmit rate from bits 62 to identify the special symbols at the start of each ATM cell and to determine the symbol that is the last in the message. Robust transmission of this information at the start of each message allows the transmitter to dynamically modify the message format as needed from one message to the next. Should one of the format bits be corrupted by an abnormally severe noise event, the "damage" is restricted to the current message only. To operate reliably, the receiver could have a "back up" method of recognizing the end of a message such as through detecting loss of signal energy for an extended duration.

FIG. 4A is a graphical illustration representing a two (2) bit per symbol signal space constellation and the increased energy symbol of FIG. 3B. The constellation points labeled "c" represent the points in a standard 2 bit per symbol constellation. For each constellation point "c" transmitted, the effect of noise can make the point appear to a receiver to have been moved with respect to where it was when it was transmitted. The dashed circle 76 surrounding constellation point 79 represents the space within which noise may move the point and still have the point reliably decoded by the receiver. The point 79 appears in a different place at the decoder due to noise induced in the communications channel 16. Each of the points "c" have a space about which they can move and still be reliably decoded by the receiver.

The circle 77 encloses the area surrounding the origin of the in-phase (horizontal) and quadrature (vertical) axes of FIG. 4A about which an interval of silence (no constellation point) can be moved by the same additive noise that can affect signal points. This additive noise could cause the silence to be interpreted by the decoder as one of the constellation points in a two (2) bit per symbol constellation due to the overlap of the decoding discrimination threshold circles 76 and 77. As shown, the circle 76 and the circle 77 have sufficient overlap in region 73 so that silence can easily be interpreted as one of the signal points "c". Conversely, one of the signal points "c" could also be interpreted by the decoder as silence.

For efficient operation, it is desirable that the beginning and end of each transmission be robustly and precisely identified (to within one (1) symbol interval). The beginning and end of each transmission are preceded and followed by silence on the line. Because the most efficient constellation encoding cannot allocate signal space to silence, it is impractical to reliably discriminate silence from signal when analyzing only a single symbol. In other words, it would be undesirable for silence that occurs before a message or after

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a message to be interpreted as a constellation point "c", and it would be undesirable for a constellation point "c" to be interpreted as silence. As mentioned above, this is possible due to the effect of noise altering the position of the constellation signal points "c" or the position of silence.

In accordance with an aspect of the invention, the first symbol (symbol 55 of FIG. 3B) in the preamble 40 is transmitted with increased energy, thereby increasing the probability that it will be reliably detected by the decoder of the receiving device. In this manner, the beginning of each transmission is clearly and robustly delimited. The signal point "b" in FIG. 4A is an exemplar one of four (4) two (2) bit per symbol constellation points that are transmitted at an increased energy level. While other increases may provide useful, a 3 dB increase is typically sufficient and does not increase the ratio of peak power to average power (PAR) of the transmitted signal. As illustrated, the signal point "b" is enclosed by dotted circle 78, within which the point "b" may move due to noise on the communication channel 16 and still be reliably decoded by the receiver. As shown, there is no overlap between circle 78 and circle 77. Accordingly, by boosting the energy of the first symbol (symbol 55 of FIG. 3B) transmitted in a communication message (31 of FIG. 3A), there is a significantly higher probability that the boosted symbol will be reliably decoded and not be mistaken for silence. Nor will silence be mistaken for this boosted energy first symbol. Preferably, the receiver places the threshold to discriminate signal from noise at one unit from the origin as shown by circle 77 in FIG. 4A.

FIG. 4B is a graphical illustration showing an exemplar grouping of constellation points representing different bit per symbol rates in accordance with an aspect of the invention. For example purposes only, assuming that normal data is encoded at five (5) bits per symbol, the black constellation points, an exemplar of one of which is illustrated using reference numeral 81, represent data encoded at five (5) bits per symbol. In accordance with an aspect of the invention, all the symbols in the preamble 40 are encoded at a rate of two (2) bits per symbol and are illustrated by the four (4) constellation points labeled "c" in FIG. 4B. These two (2) bit per symbol constellation points provide a higher signal-to-noise ratio (high margin) than do the normal data encoded at five (5) bits per symbol. This increased margin increases the probability that the receiver will reliably decode all the symbols in the preamble.

In accordance with another aspect of the invention, the four constellation points labeled "b" in FIG. 4B represent the first symbol (symbol 55 of FIGS. 3A and 3B), which energy is boosted by 3 dB. In this manner, the constellation points "b" representing the boosted symbol 55 of FIG. 3A and 3B will robustly and reliably communicate the beginning of a transmission. Circle 82 represents the maximum signal level of any symbols as the number of bits per symbol becomes arbitrarily large, but the average power of the transmitted signal is the same as it is for either the five (5) bits per symbol (81) or the two (2) bits per symbol (points "c") constellations shown. Therefore, as illustrated by circle 82, the instantaneous power required by the boosted symbol points "b" is not any higher than that used to send the normal data at any bits per symbol value. In this manner, the boosted symbol represented by constellation points "b" can be used to reliably indicate the start of a message without requiring a higher transmit level capability than that needed for normal data transmission. The non-boosted two (2) bit per symbol constellation points indicated as "c" (having a significantly higher signal-to-noise ratio than that of the normal five (5) bit per symbol data) are used to transmit all symbols of the preamble after the first symbol.

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FIG. 5 is a schematic view illustrating the communication message 31 of FIG. 3A and another aspect of the invention. Typically, it is desirable to scramble all the data bits in a communications message using a self-synchronizing scrambler so that all points in the signal constellation can be used. Unfortunately, the self-synchronizing capability of the scrambler carries the inherent disadvantage of error propagation and extension. A single bit in error in the received data stream is typically transformed by the self-synchronizing descrambling process into at least 3 erroneous bits that are separated by several bits that are not in error.

Typically, in switched-carrier operation, the scrambler setting (state) at the end of one transmission is preserved and used to begin scrambling the next message. (This enables full randomization of the encoding process so as to make full use of the available channel bandwidth.) Similarly, in a receiving device, when descrambling, the state of the descrambler that exists at the end of the previously received message is used to begin the descrambling process for the next received message. This means that the last state of the scrambler saved after scrambling the data portion of the message would then be used to begin scrambling the preamble bits of the next message.

Unfortunately, using this technique with the robust preamble 40 of the invention can lead to error propagation from the data portion of the communication message to the preamble 40. Allowing errors, which are more likely due to the larger number of bits per symbol, in the payload data to corrupt the data in the preamble due to the inherent error extension of the descrambling process significantly reduces the robustness of the preamble 40. In accordance with another aspect of the invention, a first scrambler can be used to scramble the information contained in the preamble 40 and a second scrambler can be used to scramble the data (i.e., the information in the ATM cells 44, 45, etc.)

As shown in FIG. 5, line 87 indicates that a first scrambler is used to scramble the preamble 40 of communication message 31 and also used to scramble the preamble of communication message 86. Similarly, line 88 indicates that a second scrambler is used to scramble the data portion of communication message 31 and the data portion of communication message 86. The message to message randomizing desirable for full usage of the available channel bandwidth can be maintained if the setting of the preamble scrambler (to be described with respect to FIG. 8) at the end of one preamble is used to begin the scrambling of the preamble of the next communication message 86. Because errors in the preamble are considered unlikely to occur, and because the bits received at the end of a previous preamble define the descrambler state used to descramble the next preamble, error extension from one message preamble into the preamble is also much less likely than in the single scrambler case.

An alternative to this that avoids the use of two scramblers is to save the state of the preamble scrambler after scrambling the preamble as the state to use to begin scrambling of the next preamble. This can be done instead of the conventional approach of using the state of the scrambler at the end of the message. This technique can also prevent errors at the end of one message from corrupting the preamble of the next transmission.

FIG. 6 is a schematic view illustrating the communication message 31 and the reduced line turn around delay made possible by an aspect of the invention. In time-domain duplex operation any periods during which no transceiver is transmitting represent loss of available bandwidth. To make

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most efficient usage of a communication line, it is desirable to minimize these periods. Some intervals of silence necessarily occur between transmissions because the transition from silence to the first symbol of the preamble is the manner in which the beginning of the next transmission is delimited. The process by which a transceiver makes the transition from receiving to transmitting is referred to as "line turn-around" and the time required may determine the minimum amount of silence that can occur between messages. Various aspects of the design and implementation of a time-domain duplex transceiver may result in increased delays in the line turn-around process. For example, transmitter filters and receiver equalizers have inherent delays. The analog-to-digital and digital-to-analog conversion process as well as the process of transferring digital samples between the signal processor and converters may have some inherent delays. If the signal processing is implemented in firmware there may be delays between the arrival of received signal samples and the time the processing can be performed. All of these factors may extend the line turn-around time to the point that transmission efficiency is significantly reduced.

As described above with respect to FIG. 3A, communication message 31 includes a specially encoded symbol 60 transmitted at a lower bit per symbol rate than that of the normal data encoding rate. The symbol encodes an additional bit 61 that indicates whether or not the ATM cell is the last cell in the communication message 31. If it is indicated to the receiver at the beginning of the last ATM cell 46 that the ATM cell 46 is the last cell in the communication message, (instead of waiting to the end of the ATM cell 46) line turn around delay can be reduced. As illustrated, if a receiving device must wait until the end of the last message to learn that the message is complete, there will be a delay "d" between the time that the communication message 31 is received and the time at which the transmission of communication message 91a can begin. By having advance notification that the communication message is about to be complete, a remote DSL transceiver 150 can begin transmission of the next message before reception of the current message has been completed. By knowing the delay contributed by the factors such as those mentioned previously, the transceiver can begin the transmission process, indicated by communication message 91b, so as to reduce delay "d" as much as possible, potentially reducing it to the minimum value needed for the receiver to reliably detect the transition from silence to signal at the beginning of the next message.

FIG. 7 is a block diagram illustrating the control DSL transceiver 100 of FIG. 1. Although, described with respect to control DSL transceiver 100, the following description is equally applicable to a remote DSL transceiver 150. Control DSL transceiver 100 includes microprocessor 101, memory 102, transmitter 115 and receiver 120 in communication via logical interface 108. A bi-directional stream of ATM cells from a DTE is communicated via line 14 to the control DSL transceiver 100. Memory 102 includes end of transmission delimiting software 106 and robust preamble software 104. This software resides in memory 102 and executes in microprocessor 101 in order to achieve and perform the benefits of the present invention. Transmitter 115 communicates with line interface 109 via connection 112 in order to gain access to communication channel 16. Information received on communication channel 16 is processed by line interface 109 and sent via connection 111 to receiver 120.

Transmitter 115 includes, among other elements that are known to those having ordinary skill in the art, encoder 200 and modulator 117. Similarly, receiver 120 includes, among

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other elements that have been omitted for clarity, decoder 300 and demodulator 118.

FIG. 8 is a block diagram illustrating the encoder 208 of FIG. 7. The transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the first two (2) bits of the four (4) bits (62 of FIG. 3B) that define the current transmit rate from transmit rate element 206, via connection 212. This symbol is then forwarded to preamble scrambler 217, via connection 216 for scrambling, and is then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219. This encoded symbol is then forwarded via connection 226 to gain increase element 227 where its energy is increased by approximately 3 dB and is then sent via connection 228 to multiplexer 224 and over connection 254 to modulator 117.

The next two (2) bits of the transmit rate (62 of FIG. 3B) are then scrambled and encoded in the same way. Next, the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the four (4) bits representing the requested received rate from receive rate element 204, which bits are forwarded to multiplexer 214 via connection 211. These four (4) bits are then forwarded to preamble scrambler 217 where they are scrambled, and then forwarded via connection 218 to two (2) bit per symbol preamble encoder 219 where they are encoded into a pair of symbols. These encoded symbols are forwarded directly via connection 226 to multiplexer 224 and then forwarded via connection 254 to modulator 117.

If there are multiple remote DSL transceivers 150 and 155, then the transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the two (2) bits representing the remote address from remote address element 202, which bits are then forwarded via connection 209 to multiplexer 214. These two (2) bits are then forwarded via connection 216 to preamble scrambler 217, which scrambles the bits and forwards them via connection 218 to the two (2) bit per symbol preamble encoder 219. The two (2) bit per symbol preamble encoder 219 encodes the bits and transfers the encoded symbol via connection 226 through multiplexer 224 and then via connection 254 to modulator 117.

Transmit sequencer 236 senses if an administrative header 42 and/or ATM cells 44, 45, 46 are available for transmission via connections 232 and 234, respectively, and uses this information to prepare the message format indicator which is loaded by the transmit sequencer 236 via connection 207. The transmit sequencer 236 commands the multiplexer 214 via connection 242 to select the two (2) bits representing the message format from element 201, which bits are then forwarded via connection 208 to multiplexer 214. These two (2) bits are then forwarded via connection 216 to preamble scrambler 217, which scrambles the bits and forwards them via connection 218 to the two (2) bit per symbol preamble encoder 219. The two (2) bit per symbol preamble encoder 219 encodes the bits and transfers the encoded symbol via connection 226 through multiplexer 224 and then via connection 254 to modulator 117.

Next, transmission of either the administrative header 42 or the ATM cell payload begins by transmit sequencer 236 sending a command via connection 235 to multiplexer 241 to select either the administrative header 42 via element 229 or payload data via element 231. These bits are supplied through multiplexer 241 via connections 239 and 238 and are then forwarded via connection 244 to payload scrambler 246. Payload scrambler 246 scrambles the bits and forwards them via connection 248 to N bit per symbol data encoder 249 and N-1 bit per symbol data encoder 251. As mentioned

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above with respect to FIG. 5, payload scrambler 246 may use as its initial state either the state that exists at the end of scrambling the preamble (supplied via connection 247) or the state that exists after completion of scrambling the payload portion of the previous message. As mentioned above with respect to FIG. 3A, all the data bits are encoded at an N bit per symbol data rate by data encoder 249 and forwarded via connection 257 to multiplexer 224 until the first symbol containing only bits from a new ATM cell is detected. This symbol is encoded at a rate of N-1 bits per symbol by N-1 bit per symbol data encoder 251 and forwarded via connection 256 to multiplexer 224. The index for this symbol as delivered to payload scrambler 246 is formed by selecting the first N-2 bits of the first octet of the cell and adding an additional bit (i.e., bit 54 or bit 61 of FIG. 3A) representing the state of the last cell signal 237 as selected via multiplexer 241. When instructed by transmit sequencer 236 via connection 252, the multiplexer 224 selects the symbols from either N bit per symbol data encoder 249 or from N-1 bit per symbol data encoder 251 and forwards these symbols via connection 254 to modulator 117.

Transmit sequencer 236 uses the payload bits per symbol value N received via connection 212 to determine the number of symbols to encode for each cell and to determine which symbol is to be encoded at the N-1 bits per symbol rate and contain the last cell indicator bit. After completing transmission of the message, transmit sequencer 236 commands multiplexer 224 via connection 252 to select silence 221 via connection 222 as the input to the modulator 117.

FIG. 9 is a block diagram illustrating the decoder 300 of FIG. 7. A received transmission stream is received in demodulator 118, where it is demodulated in accordance with techniques known to those having ordinary skill in the art. The first symbol is forwarded via connection 301 to gain reduction element 302. Gain reduction element 302 reduces the gain of the first symbol and supplies that reduced energy symbol via connection 304 to multiplexer 306. Receive sequencer 328 sends a signal to multiplexer 306 via connection 354 instructing multiplexer 306 to select that reduced gain symbol and transfer it via connection 307 to two (2) bit per symbol preamble decoder 308. The decoded bits from the first symbol are then sent via connection 309 to preamble descrambler 311. Preamble descrambler 311 descrambles the first bits in the transmission and forwards them via connection 312 to the multiplexer 314. When instructed by receive sequencer 328 via connection 332, the multiplexer 314 forwards these bits via connection 324 to transmit rate element 236.

The following preamble symbols are all forwarded via connection 301 directly to multiplexer 306, which forwards these symbols via connection 307 for decoding by two (2) bit per symbol preamble decoder 308. The decoded bits are forwarded via connection 309 to preamble descrambler 311 as mentioned above. These bits are then forwarded in order via connections 324, 321, 318 and 316 to transmit rate element 326, receive rate element 322, remote address element 319 and message format element 317, respectively.

Next, the administrative header symbols and ATM cell data symbols that have been encoded at N bits per symbol are forwarded via connection 301 to N bit per symbol data decoder 337 and the ATM cell data symbols that have been encoded at N-1 bits per symbol are forwarded via connection 301 to N-1 bit per symbol data decoder 339. These symbols are decoded and the decoded bits are transferred via connections 338 and 341 to multiplexer 342. Similarly, as mentioned above with respect to FIG. 8, receive sequencer

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328 insures that the symbols encoded at the rate of  $N-1$  bits per symbol are forwarded via connection 301 to  $N-1$  bit per symbol data decoder 339, which forwards the decoded bits via connection 341 to multiplexer 342. As shown, the value of  $N$ , which is the bits per symbol value used for the  $N$  bits per symbol, or  $N-1$  bits per symbol decoding is controlled by the just received transmit rate bits that have been stored in transmit rate element 326.

At the appropriate time, receive sequencer 328 commands the multiplexer 342 via connection 347 to forward the bits via connection 344 to payload descrambler 336. In accordance with an aspect of the invention, the preamble descrambler 311 operates only on the preamble bits and the payload descrambler 336 operates only on the payload bits. As mentioned above with respect to FIG. 5, the payload descrambler may use as its initial state either the state of the preamble descrambler at the end of descrambling the preamble as supplied via connection 334 or the state of the payload descrambler at the end of descrambling the payload bits of the previous message. The descrambled payload bits are then forwarded via connection 346 to multiplexer 349. When ordered by receive sequencer 328 via connection 331, the multiplexer 349 forwards the administrative header bits via connection 351 and the payload data bits via connection 352. These bits are then forwarded via logical interface 108 to microprocessor 101 for processing (FIG. 7). Receive sequencer 328 determines the presence or absence of the administrative header and ATM cells via the just received message format bits that have been stored in element 317 and provided to receive sequencer 328 via connection 327. When the bits for each symbol containing the last message bit are available at multiplexer 349, receive sequencer 328 directs the  $N-2$  bits of payload data to the payload data element 356 via connection 352 and receives the last cell bit via connection 329. Receive sequencer 328 uses the current bits per symbol value for payload data received via connection 324 to determine the beginning and end of each cell. Based on the message format and the value of the last cell indicator bit, receive sequencer 328 determines when the last symbol of the message has been decoded and instructs demodulator 118 (FIG. 7) to stop delivering demodulated symbols.

In an alternative embodiment, the special encoding of the last cell as described above in FIG. 3A can be omitted and an "eye pattern closure test" can be used to detect the end of the message. In such a situation where it is acceptable to lose the advanced notification of the end of the transmission, beneficial alternative uses for the special encoding of the first bits of each cell are possible. For example, this special encoding as described above with respect to FIG. 3A wherein  $N-2$  bits are encoded for the first full bytes of each cell, can be used to indicate whether or not the ATM cell header (e.g., ATM header 47 of FIG. 2B) is present. This can be useful in the situation in which a string of ATM cells have exactly the same header. This can happen, for example, for ATM adaptation layer 5 (AAL5) cells that carry data from a single protocol data unit (PDU) if no other cells have been interleaved. The single extra bit (bit 61 of FIG. 3A) provided by the encoding described above with respect to FIG. 3A, can be used to indicate whether or not the following cell contains a header. If the bit 61 indicates that there is no header, the receiver copies the last header received ahead of the payload octets of this next cell before forwarding it to the ATM layer. Advantageously, this reduces the approximate 10 percent overhead imposed by the five (5) octet header (47 of FIG. 2B).

It should be emphasized that the above-described embodiments of the present invention, particularly any "preferred"

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embodiments, are merely possible examples of implementations, merely set forth for a clear understanding of the principles of the invention. Many variations and modifications may be made to the above-described embodiment(s) of the invention without departing substantially from the spirit and principles of the invention. For example, the robust preamble and transmission delimiting system and method are applicable in all switched-carrier transmission methodologies in which it is desirable to reliably convey channel establishment information and reliably delimit the beginning and end of each communication message. All such modifications and variations are intended to be included herein within the scope of the present invention.

Therefore, having thus described the invention, at least the following is claimed:

1. A system for robust transmission delimiting, comprising:

a communication message including a preamble, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

an encoder configured to encode the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel.

2. A system for robust transmission delimiting, comprising:

a communication message including a preamble, the preamble including a plurality of bits representing communication link control information; and

an encoder configured to encode the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being supported over a communication channel,

wherein the preamble includes information that defines a rate at which data following the preamble has been encoded for transmission.

3. The system as defined in claim 2, further comprising a gain boost element configured to increase the energy of the first symbol index to reliably indicate the beginning of the communication message.

4. The system as defined in claim 2, wherein the preamble includes information defining a maximum rate at which a first transceiver that is sending the preamble is able to receive transmissions from a second transceiver that is receiving the preamble.

5. The system as defined in claim 2, wherein the preamble indicates whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

6. The system as defined in claim 2, wherein the preamble indicates whether administrative information follows the preamble.

7. The system as defined in claim 5, further comprising:

a first scrambler configured to scramble the preamble; and

a second scrambler configured to scramble the data, wherein a state of the scrambler used to scramble the bits that comprise the preamble is the state that existed when scrambling of a previous preamble was completed.

8. The system as defined in claim 5, wherein the data portion of the communication message comprises fixed size units, the fixed size units comprising a plurality of bits and

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wherein the bits are encoded into symbol indices such that, for each of the fixed size units, one symbol index is encoded differently from the other symbols.

9. The system as defined in claim 8, wherein the differently encoded symbol index further comprises an extra bit that indicates whether the fixed size unit from which the other bits of the differently encoded symbol indices are obtained is the last one transmitted in a message.

10. The system as defined in claim 8, wherein the differently encoded symbol index is encoded at a data rate lower than that of the other symbols carrying message data.

11. A system for delimiting the end of a transmission, comprising:

a communication message segmented into a plurality of fixed size units, each fixed size unit including a plurality of bits; and

an encoder configured to encode the plurality of bits into a plurality of symbol indices at a first data rate, the encoder also configured to encode at a second rate when producing the first symbol index in the plurality of symbol indices that contains only bits from each fixed size unit, where the second rate is lower than the first rate.

12. A method for robust transmission delimiting, the method comprising the steps of:

applying a preamble to a communication message, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

13. A method for robust transmission delimiting, the method comprising the steps of:

applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information;

encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel; and including information in the preamble defining a rate at which data following the preamble has been encoded for transmission.

14. The method as defined in claim 13, further comprising the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

15. The method as defined in claim 13, further comprising the step of including information in the preamble defining a maximum rate at which a transceiver that is sending the preamble is able to receive transmissions from a transceiver that is receiving the preamble.

16. The method as defined in claim 13, further comprising the step of using the preamble to indicate whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

17. The method as defined in claim 13, further comprising the step of using the preamble to indicate whether administrative information follows the preamble.

18. The method as defined in claim 16, further comprising the steps of:

scrambling the preamble using a first scrambler; and scrambling the data using a second scrambler; and

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scrambling the bits in the preamble using the state of the scrambler that existed when scrambling of the previous preamble was complete.

19. The method as defined in claim 16, wherein the data portion of the communication message comprises fixed size units, the fixed size units comprising a plurality of bits, and wherein the bits that comprise each of the fixed size units are encoded into symbol indices such that for each of the fixed size units, one symbol index is encoded differently from the other symbols.

20. The method as defined in claim 19, further comprising the step of including in said differently encoded symbol index an extra bit that indicates whether the fixed size unit from which the other bits of said differently encoded symbol indices are obtained is the last one transmitted in a message.

21. The method as defined in claim 19, further comprising the step of encoding the differently encoded symbol index at a data rate lower than that of the other symbols carrying message data.

22. A method for delimiting the end of a transmission, the method comprising the steps of:

segmenting a communication message into a plurality of units, each unit including a plurality of bits and having a fixed size;

encoding a plurality of the bits in the plurality of units into a plurality of symbol indices, the symbol indices being encoded at a first rate; and

encoding one symbol index of the plurality of symbol indices at a rate lower than the first rate, the one symbol index containing bits from only one of the plurality of units.

23. A system for robust transmission delimiting, comprising:

means for applying a preamble to a communication message, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

means for encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

24. The system as defined in claim 23, further comprising means for increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

25. A system for robust transmission delimiting, comprising:

means for applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information;

means for encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel; and

means for including information in the preamble defining a rate at which data following the preamble has been encoded for transmission.

26. The system as defined in claim 23, further comprising means for including information in the preamble defining a maximum rate at which a transceiver that is sending the preamble is able to receive transmissions from a transceiver that is receiving the preamble.

27. The system as defined in claim 23, further comprising means for using the preamble to indicate whether a data

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portion follows the preamble and, if so, the format and type of data that follows the preamble.

28. The system as defined in claim 23, further comprising means for using the preamble to indicate whether administrative information follows the preamble.

29. The system as defined in claim 27, further comprising:  
means for scrambling the preamble using a first scrambler;

means for scrambling the data using a second scrambler; and

means for scrambling the bits in the preamble using the state of the scrambler that existed when scrambling of the previous preamble was complete.

30. The system as defined in claim 27, wherein the data portion of the communication message comprises fixed size units, the fixed size units comprising a plurality of bits; and means for encoding the bits that comprise each of the fixed size units into symbol indices such that for each of the fixed size units, one symbol index is encoded differently from the other symbols.

31. The system as defined in claim 30, further comprising means for including in said differently encoded symbol index an extra bit that indicates whether the fixed size unit from which the other bits of said differently encoded symbol indices are obtained is the last one transmitted in a message.

32. The system as defined in claim 30, further comprising means for encoding the differently encoded symbol index at a data rate lower than that of the other symbols carrying message data.

33. A system for delimiting the end of a transmission, comprising:

means for segmenting a communication message into a plurality of fixed size units, each unit including a plurality of bits;

means for encoding a plurality of the bits in the units into a plurality of symbol indices, the symbol indices being encoded at a first rate; and

means for encoding at a second rate when producing the first symbol index in the plurality of symbol indices that contains only bits from each fixed size unit, where the second rate is lower than the first rate.

34. A computer readable medium having a program for robust transmission delimiting, the program comprising logic for performing the steps of:

applying a preamble to a communication message, the preamble operating to frame the message and to delimit the message from silence, the preamble including a plurality of bits representing communication link control information; and

encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per symbol rate relative to the maximum rate capable of being transmitted over a communication channel.

35. The program as defined in claim 34, further comprising logic for performing the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

36. A computer readable medium having a program for robust transmission delimiting, the program comprising logic for performing the steps of:

applying a preamble to a communication message, the preamble including a plurality of bits representing communication link control information;

encoding the preamble bits into a plurality of symbol indices, the symbol indices encoded at a lower bit per

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symbol rate relative to the maximum rate capable of being transmitted over a communication channel; and including information in the preamble defining a rate at which data following the preamble has been encoded for transmission.

37. The program as defined in claim 36, further comprising logic for performing the step of including information in the preamble defining a maximum rate at which a transceiver that is sending the preamble is able to receive transmissions from a transceiver that is receiving the preamble.

38. The program as defined in claim 36, further comprising logic for performing the step of using the preamble to indicate whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

39. The program as defined in claim 36, further comprising logic for performing the step of using the preamble to indicate whether administrative information follows the preamble.

40. The program as defined in claim 38, further comprising logic for performing the steps of:

scrambling the preamble using a first scrambler;

scrambling the data using a second scrambler; and

scrambling the bits in the preamble using the state of the scrambler that existed when scrambling of the previous preamble was complete.

41. The program as defined in claim 38, wherein the data portion of the communication message comprises fixed size units, the fixed size units comprising a plurality of bits; and wherein the bits that comprise each of the fixed size units are encoded into symbol indices such that for each of the fixed size units, one symbol index is encoded differently from the other symbols.

42. The program as defined in claim 41, further comprising logic for performing the step of including in said differently encoded symbol index an extra bit that indicates whether the fixed size unit from which the other bits of said differently encoded symbol indices are obtained is the last one transmitted in a message.

43. The program as defined in claim 41, further comprising logic for performing the step of encoding the differently encoded symbol index at a data rate lower than that of the other symbols carrying message data.

44. A computer readable medium having a program for delimiting the end of a transmission, the program comprising logic to perform the steps of:

segmenting a communication message into a plurality of fixed size units, each unit including a plurality of bits;

encoding a plurality of the bits in the fixed sized units into a plurality of symbol indices, the symbol indices being encoded at a first rate; and

encoding at a second rate when producing the first symbol index in the plurality of symbol indices that contains only bits from each fixed size unit, where the second rate is lower than the first rate.

45. A method for delimiting the end of a transmission, the method comprising the steps of:

segmenting a communication message into a plurality of fixed size units, each unit including a plurality of bits;

encoding the first N bits in a unit into a first symbol index, the first symbol index being encoded at a first rate, N being less than the fixed size; and

encoding the remaining bits in the plurality of units into a plurality of symbol indices at a rate greater than the first rate.

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46. The system as defined in claim 11, further comprising a gain boost element configured to increase the energy of the first symbol index to reliably indicate the beginning of the communication message.

47. The system as defined in claim 11, wherein the preamble indicates whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

48. The method as defined in claim 22, further comprising the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

49. The method as defined in claim 22, further comprising the step of using the preamble to indicate whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

50. The system as defined in claim 33, further comprising means for increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

51. The system as defined in claim 33, further comprising means for using the preamble to indicate whether a data

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portion follows the preamble and, if so, the format and type of data that follows the preamble.

52. The program as defined in claim 44, further comprising logic for performing the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

53. The program as defined in claim 44, further comprising logic for performing the step of using the preamble to indicate whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

54. The method as defined in claim 45, further comprising the step of increasing the energy of the first symbol index to reliably indicate the beginning of the communication message.

55. The method as defined in claim 45, further comprising the step of using the preamble to indicate whether a data portion follows the preamble and, if so, the format and type of data that follows the preamble.

\* \* \* \* \*

**Exhibit C**

Thomas J. Meloro (TM-7668)  
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Tel: (212) 728-8000

UNITED STATES BANKRUPTCY COURT  
SOUTHERN DISTRICT OF NEW YORK

In re Adelphia Communications Corporation,  
et al.,

Debtors.

Chapter 11

Case No. 02-41729 (REG)  
(Jointly Administered)

Rembrandt Technologies, LP,

Plaintiff/Counter-defendants,

V.

Adversary Proceeding  
No. 06-01739 (REG)

Adelphia Communications Corporation;  
Century-TCI California, LP;  
Century-TCI California Communications, LP;  
Century-TCI Distribution Company, LLC;  
Century-TCI Holdings, LLC;  
Parnassos, LP;  
Parnassos Communications, LP;  
Parnassos Distribution Company I, LLC;  
Parnassos Distribution Company II, LLC;  
Parnassos Holdings, LLC; and  
Western NY Cablevision, LP,

### Defendants/Counterclaimants.

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**ANSWER, AFFIRMATIVE DEFENSES, AND COUNTERCLAIMS OF DEFENDANTS  
AND REORGANIZED DEBTORS IN POSSESSION ADELPHIA COMMUNICATIONS  
CORPORATION; CENTURY-TCI CALIFORNIA, LP; CENTURY-TCI CALIFORNIA  
COMMUNICATIONS, LP; CENTURY-TCI DISTRIBUTION COMPANY, LLC;  
CENTURY-TCI HOLDINGS, LLC; PARNASSOS, LP; PARNASSOS  
COMMUNICATIONS, LP; PARNASSOS DISTRIBUTION COMPANY I, LLC;  
PARNASSOS DISTRIBUTION COMPANY II, LLC; AND WESTERN NY  
CABLEVISION, LP**

Defendants and Reorganized Debtors in Possession Adelphia Communications Corporation ("Adelphia"); Century-TCI California, LP; Century-TCI California Communications, LP; Century-TCI Distribution Company, LLC; Century-TCI Holdings, LLC; Parnassos, LP; Parnassos Communications, LP; Parnassos Distribution Company I, LLC; Parnassos Distribution Company II, LLC; Parnassos Holdings, LLC; and Western NY Cablevision, LP (collectively, "Defendants"), by their attorneys Willkie Farr & Gallagher LLP, for their answer to the Complaint for Post-Petition Patent Infringement (the "Complaint"), state as follows:

**AS TO THE PARTIES**

1. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 1 of the Complaint.
2. Deny the allegations contained in paragraph 2 of the Complaint, except admit that (i) Adelphia is a corporation incorporated under the laws of Delaware having its principal place of business in Greenwood Village, Colorado; (ii) on June 25, 2002, Adelphia had its principal place of business in Coudersport, Pennsylvania; (iii) Adelphia filed a voluntary petition under chapter 11 of title 11 of the United States Code in the United States Bankruptcy Court for the Southern District of New York on June 25, 2002, and its Chapter 11 case is captioned *In re Adelphia Communications Corporation*, Case No. 02-41729 (REG); (iv) Adelphia's Chapter 11

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case is pending; and (v) prior to the sale of substantially all of their assets on July 31, 2006, Defendants and their affiliates served customers in 31 states and offered analog and digital video services, high-speed Internet access and other advanced services over its broadband networks.

3. Admit the allegations contained in paragraph 3 of the Complaint, except deny that Century-TCI California, LP is an affiliate of Adelphia.

4. Admit the allegations contained in paragraph 4 of the Complaint, except deny that Century-TCI California Communications, LP is an affiliate of Adelphia.

5. Admit the allegations contained in paragraph 5 of the Complaint.

6. Admit the allegations contained in paragraph 6 of the Complaint, except deny that Century-TCI Holdings, LLC is an affiliate of Adelphia.

7. Admit the allegations contained in paragraph 7 of the Complaint, except deny that Parnassos Communications, LP is an affiliate of Adelphia.

8. Admit the allegations contained in paragraph 8 of the Complaint.

9. Admit the allegations contained in paragraph 9 of the Complaint.

10. Admit the allegations contained in paragraph 10 of the Complaint, except deny that Parnassos Holdings, LLC is an affiliate of Adelphia.

11. Admit the allegations contained in paragraph 11 of the Complaint, except deny that Parnassos, LP is an affiliate of Adelphia.

12. Admit the allegations contained in paragraph 12 of the Complaint, except deny that Western NY Cablevision, LP is an affiliate of Adelphia.

13. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 13 of the Complaint, except deny that Defendants are liable for patent infringement as alleged.

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**AS TO JURISDICTION AND VENUE**

14. Admit that Plaintiff purports that this is an action for patent infringement arising under the laws of the United States relating to patents, including, *inter alia*, 35 U.S.C. §§ 271, 281, 284, and 285. Admit that this Court has jurisdiction over such claims pursuant to 28 U.S.C. §§ 1331 and 1338(a).

15. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 15 of the Complaint, except admit that prior to the sale of substantially all of their assets on July 31, 2006, Defendants and their affiliates served customers in 31 states and offered analog and digital video services, high-speed Internet access and other advanced services over its broadband networks, and deny that Defendants engaged in post-petition acts of patent infringement that have damaged Plaintiff.

16. Deny the allegations contained in paragraph 16 of the Complaint, except admit that Defendants have submitted to the jurisdiction of this Court in the bankruptcy proceedings.

17. Deny the allegations contained in paragraph 17 of the Complaint, except admit that venue is proper pursuant to 28 U.S.C. § 1409(a).

**AS TO COUNT I**

18. In response to paragraph 18 of the Complaint, Defendants repeat and reallege paragraphs 1 through 17 with the same force and effect as if fully set forth herein.

19. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 19 of the Complaint, except admit that U.S. Patent No. 5,710,761 (the "'761 patent") is entitled "Error Control Negotiation Based on Modulation" and that a copy of the '761 patent is attached to the Complaint as Exhibit A.

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20. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 20 of the Complaint.

21. Deny the allegations contained in paragraph 21 of the Complaint.

22. Deny the allegations contained in paragraph 22 of the Complaint.

**AS TO COUNT II**

23. In response to paragraph 23 of the Complaint, Defendants repeat and reallege paragraphs 1 through 17 with the same force and effect as if fully set forth herein.

24. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 24 of the Complaint, except admit that U.S. Patent No. 5,778,234 (the "'234 patent") is entitled "Method for Downloading Programs" and that a copy of the '234 patent is attached to the Complaint as Exhibit B.

25. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 25 of the Complaint.

26. Deny the allegations contained in paragraph 26 of the Complaint.

27. Deny the allegations contained in paragraph 27 of the Complaint.

**AS TO COUNT III**

28. In response to paragraph 28 of the Complaint, Defendants repeat and reallege paragraphs 1 through 17 with the same force and effect as if fully set forth herein.

29. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 29 of the Complaint, except admit that U.S. Patent No. 6,131,159 (the "'159 patent") is entitled "System for Downloading Programs" and that a copy of the '159 patent is attached to the Complaint as Exhibit C.

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30. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 30 of the Complaint.

31. Deny the allegations contained in paragraph 31 of the Complaint.

32. Deny the allegations contained in paragraph 32 of the Complaint.

#### **AS TO COUNT IV**

33. In response to paragraph 33 of the Complaint, Defendants repeat and reallege paragraphs 1 through 17 with the same force and effect as if fully set forth herein.

34. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 34 of the Complaint, except admit that U.S. Patent No. 6,950,444 (the "'444 patent") is entitled "System and Method for a Robust Preamble and Transmission Delimiting in a Switched-Carrier Transceiver" and that a copy of the '444 patent is attached to the Complaint as Exhibit D.

35. Deny knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 35 of the Complaint.

36. Deny the allegations contained in paragraph 36 of the Complaint.

37. Deny the allegations contained in paragraph 37 of the Complaint.

WHEREFORE, Defendants pray that Plaintiff take nothing by its causes of action or for its costs and pray for such other relief as the Court deems just and proper.

#### **FULL AND COMPLETE DEFENSES**

##### **FIRST FULL AND COMPLETE DEFENSE**

The Complaint and each purported cause of action set forth in the Complaint fail to state a claim upon which relief can be granted.

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SECOND FULL AND COMPLETE DEFENSE

Plaintiff's claims are barred, in whole or in part, to the extent they have been asserted beyond the time allowed by the applicable statute of limitations.

THIRD FULL AND COMPLETE DEFENSE

None of the acts or omissions alleged in the Complaint proximately caused, in whole or in part, any alleged injury that the Complaint seeks to redress.

FOURTH FULL AND COMPLETE DEFENSE

Plaintiff is estopped from asserting each of the purported causes of action set forth in the Complaint.

FIFTH FULL AND COMPLETE DEFENSE

Plaintiff has waived any right to assert each of the purported causes of action set forth in the Complaint.

SIXTH FULL AND COMPLETE DEFENSE

With respect to each purported cause of action set forth in the Complaint, Plaintiff has failed to mitigate its damages.

SEVENTH FULL AND COMPLETE DEFENSE

Each of the purported causes of action set forth in the Complaint is barred by the doctrine of unclean hands.

EIGHTH FULL AND COMPLETE DEFENSE

Each of the purported causes of action set forth in the Complaint is barred by the doctrine of laches.

NINTH FULL AND COMPLETE DEFENSE

Each of the purported causes of action set forth in the Complaint are in violation of the automatic stay provisions of 11 U.S.C. § 362(a).

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TENTH FULL AND COMPLETE DEFENSE

The '761, '234, '159, and '444 patents are invalid for failure to comply with the conditions set forth in 35 U.S.C. §§ 101 *et seq.*

ELEVENTH FULL AND COMPLETE DEFENSE

Plaintiff has failed to plead which, if any, of Defendants' products are alleged to infringe the '761, '234, '159, and '444 patents. Defendants have not infringed, contributorily infringed, or induced the infringement of any valid claim of the '761, '234, '159, and '444 patents, either literally or under the doctrine of equivalents.

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**COUNTERCLAIMS OF DEFENDANTS AND REORGANIZED DEBTORS IN  
POSSESSION ADELPHIA COMMUNICATIONS CORPORATION; CENTURY-TCI  
CALIFORNIA, LP; CENTURY-TCI CALIFORNIA COMMUNICATIONS, LP;  
CENTURY-TCI DISTRIBUTION COMPANY, LLC; CENTURY-TCI HOLDINGS, LLC;  
PARNASSOS, LP; PARNASSOS COMMUNICATIONS, LP; PARNASSOS  
DISTRIBUTION COMPANY I, LLC; PARNASSOS DISTRIBUTION COMPANY II,  
LLC; AND WESTERN NY CABLEVISION, LP**

**PARTIES**

1. Counterclaimant Adelphia Communications Corporation is a corporation organized under the laws of the state of Delaware.
2. Counterclaimant Century-TCI California, LP is a partnership organized under the laws of the state of Delaware.
3. Counterclaimant Century-TCI California Communications, LP is a partnership organized under the laws of the state of Delaware.
4. Counterclaimant Century-TCI Distribution Company, LLC is a limited liability company organized under the laws of the state of Delaware.
5. Counterclaimant Century-TCI Holdings, LLC is a limited liability company organized under the laws of the state of Delaware.
6. Counterclaimant Parnassos, LP is a partnership organized under the laws of the state of Delaware.
7. Counterclaimant Parnassos Communications, LP is a partnership organized under the laws of the state of Delaware.
8. Counterclaimant Parnassos Distribution Company I, LLC is a limited liability company organized under the laws of the state of Delaware.
9. Counterclaimant Parnassos Distribution Company II, LLC is a limited liability company organized under the laws of the state of Delaware.

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10. Counterclaimant Parnassos Holdings, LLC is a limited liability company organized under the laws of the state of Delaware.

11. Counterclaimant Western NY Cablevision, LP is a partnership organized under the laws of the state of Delaware.

12. Counterclaimants Adelphia Communications Corporation; Century-TCI California, LP; Century-TCI California Communications, LP; Century-TCI Distribution Company, LLC; Century-TCI Holdings, LLC; Parnassos, LP; Parnassos Communications, LP; Parnassos Distribution Company I, LLC; Parnassos Distribution Company II, LLC; Parnassos Holdings, LLC; and Western NY Cablevision, LP are collectively referred to in these counterclaims as “Adelphia.”

13. On information and belief, Rembrandt Technologies, LP (“Rembrandt”) is a limited partnership organized under the laws of the state of New Jersey, with its principal place of business at 401 City Avenue, Suite 815, Bala Cynwyd, Pennsylvania 19004.

#### **JURISDICTION AND VENUE**

14. Subject matter jurisdiction is proper under 28 U.S.C. §§ 1331 and 1338(a).

15. Venue in this district is proper for Adelphia’s counterclaims under 28 U.S.C. §§ 1391(b) and 1409(a).

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**COUNT I**

**DECLARATORY JUDGMENT OF NONINFRINGEMENT  
AND INVALIDITY OF THE '761 PATENT**

16. Adelphia incorporates by reference the allegations made in its Affirmative Defenses and in Paragraphs 1-15 above.

17. An actual controversy exists between Adelphia and Rembrandt over Adelphia's alleged infringement and invalidity of United States Patent No. 5,710,761.

18. Adelphia has not infringed, contributorily infringed, or induced the infringement of any valid claims of the '761 patent, either literally or under the doctrine of equivalents.

19. The '761 patent is invalid in light of the failure to comply with one or more requirements of 35 U.S.C. §§ 101 *et seq.*

20. Rembrandt's claims that Adelphia is infringing, contributorily infringing or actively inducing the infringement of the '761 patent render this case exceptional within the meaning of 35 U.S.C. § 285, entitling Adelphia to recover its attorney fees, costs and expenses in defending against those claims.

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**COUNT II**

**DECLARATORY JUDGMENT OF NONINFRINGEMENT  
AND INVALIDITY OF THE '234 PATENT**

21. Adelphia incorporates by reference the allegations made in its Affirmative Defenses and in Paragraphs 1-20 above.

22. An actual controversy exists between Adelphia and Rembrandt over Adelphia's alleged infringement and invalidity of United States Patent No. 5,778,234.

23. Adelphia has not infringed, contributorily infringed, or induced the infringement of any valid claims of the '234 patent, either literally or under the doctrine of equivalents.

24. The '234 patent is invalid in light of the failure to comply with one or more requirements of 35 U.S.C. §§ 101 *et seq.*

25. Rembrandt's claims that Adelphia is infringing, contributorily infringing or actively inducing the infringement of the '234 patent render this case exceptional within the meaning of 35 U.S.C. § 285, entitling Adelphia to recover its attorney fees, costs and expenses in defending against those claims.

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**COUNT III**

**DECLARATORY JUDGMENT OF NONINFRINGEMENT  
AND INVALIDITY OF THE '159 PATENT**

26. Adelphia incorporates by reference the allegations made in its Affirmative Defenses and in Paragraphs 1-25 above.

27. An actual controversy exists between Adelphia and Rembrandt over Adelphia's alleged infringement and invalidity of United States Patent No. 6,131,159.

28. Adelphia has not infringed, contributorily infringed, or induced the infringement of any valid claims of the '159 patent, either literally or under the doctrine of equivalents.

29. The '159 patent is invalid in light of the failure to comply with one or more requirements of 35 U.S.C. §§ 101 *et seq.*

30. Rembrandt's claims that Adelphia is infringing, contributorily infringing or actively inducing the infringement of the '159 patent render this case exceptional within the meaning of 35 U.S.C. § 285, entitling Adelphia to recover its attorney fees, costs and expenses in defending against those claims.

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**COUNT IV**

**DECLARATORY JUDGMENT OF NONINFRINGEMENT  
AND INVALIDITY OF THE '444 PATENT**

31. Adelphia incorporates by reference the allegations made in its Affirmative Defenses and in Paragraphs 1-30 above.

32. An actual controversy exists between Adelphia and Rembrandt over Adelphia's alleged infringement and invalidity of United States Patent No. 6,950,444.

33. Adelphia has not infringed, contributorily infringed, or induced the infringement of any valid claims of the '444 patent, either literally or under the doctrine of equivalents.

34. The '444 patent is invalid in light of the failure to comply with one or more requirements of 35 U.S.C. §§ 101 *et seq.*

35. Rembrandt's claims that Adelphia is infringing, contributorily infringing or actively inducing the infringement of the '444 patent render this case exceptional within the meaning of 35 U.S.C. § 285, entitling Adelphia to recover its attorney fees, costs and expenses in defending against those claims.

**PRAYER FOR RELIEF**

For the reasons set forth above, Adelphia prays for the Court's judgment that:

- (i) the '761, '234, '159 and '444 patents are invalid;
- (ii) Adelphia has not infringed, contributorily infringed, or induced the infringement of any claim of the '761, '234, '159 and '444 patents;
- (iii) Plaintiff's Complaint be dismissed with prejudice;
- (iv) Plaintiff takes nothing by reason of its claims against Adelphia;

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(v) this case is exceptional and entitles Adelphia to an award of its attorney fees, costs and expenses under 35 U.S.C. § 285; and

(vi) such other and further relief at law or equity be granted to Adelphia as the Court may deem just and proper.

Date: November 27, 2006



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*Attorneys for Defendants/Counter-Claimants  
and Reorganized Debtors in Possession  
Adelphia Communications Corporation;  
Century-TCI California, LP;  
Century-TCI California Communications, LP;  
Century-TCI Distribution Company, LLC;  
Century-TCI Holdings, LLC;  
Parnassos, LP;  
Parnassos Communications, LP;  
Parnassos Distribution Company I, LLC;  
Parnassos Distribution Company II, LLC;  
Parnassos Holdings, LLC;  
Western NY Cablevision, LP*

**Exhibit D**

Vineet Bhatia (VB 9964)  
 SUSMAN GODFREY L.L.P.  
 590 Madison Ave., 8<sup>th</sup> Floor  
 New York, NY 10022  
 Main Telephone: (212) 336-8330

**UNITED STATES BANKRUPTCY COURT  
 SOUTHERN DISTRICT OF NEW YORK**

In Re: Adelphia Communications Corporation, et al.	)	Chapter 11
	)	
	)	Case No. 02-41729 (REG)
Debtors	)	Jointly Administered
	)	
Rembrandt Technologies, LP	)	
	)	Adversary Proceeding
<i>Plaintiff/Counter-defendants</i>	)	
	)	No. 06-01739 (REG)
v.	)	
	)	
Adelphia Communications Corporation;	)	
Century-TCI California, LP;	)	
Century-TCI California Communications, LP;	)	
Century-TCI Distribution Company, LLC;	)	
Century-TCI Holdings, LLC;	)	
Parnassos, LP;	)	
Parnassos Communications, LP;	)	
Parnassos Distribution Company I, LLC;	)	
Parnassos Distribution Company II, LLC;	)	
Parnassos Holdings, LLC;	)	
Western NY Cablevision, LP	)	
	)	
<i>Defendants/Counterclaimants</i>	)	

**PLAINTIFF'S REPLY TO DEFENDANTS' ANSWER AND COUNTERCLAIMS**

Plaintiff Rembrandt Technologies, LP ("Rembrandt") respectfully submits this Reply to the Answer and Counterclaims of Defendants and Reorganized Debtors in Possession Adelphia Communications Corporation; Century-TCI California, LP; Century-TCI California Communications, LP; Century-TCI Distribution Company, LLC; Century-TCI Holdings, LLC;

Parnassos, LP; Parnassos Communications, LP; Parnassos Distribution Company I, LLC; Parnassos Distribution Company II, LLC; Parnassos Holdings, LLC; and Western NY Cablevision, LP filed November 27, 2006.

**PARTIES**

1. Admitted.
2. Admitted.
3. Admitted.
4. Admitted.
5. Admitted.
6. Admitted.
7. Admitted.
8. Admitted.
9. Admitted.
10. Admitted.
11. Admitted.
12. Admitted.
13. Admitted.

**JURISDICTION AND VENUE**

14. Admitted.
15. Admitted.

**COUNT I**

16. Rembrandt repeats and re-alleges its response to paragraphs 1-15 of the Counterclaims, and further incorporates by reference its allegations in its Complaint filed September 13, 2006.

17. Admitted.

18. Denied.

19. Denied.

20. Denied.

**COUNT II**

21. Rembrandt repeats and re-alleges its response to paragraphs 1-20 of the Counterclaims, and further incorporates by reference its allegations in its Complaint filed September 13, 2006.

22. Admitted.

23. Denied.

24. Denied.

25. Denied.

**COUNT III**

26. Rembrandt repeats and re-alleges its response to paragraphs 1-25 of the Counterclaims, and further incorporates by reference its allegations in its Complaint filed September 13, 2006.

27. Admitted.

28. Denied.

29. Denied.

30. Denied.

**COUNT IV**

31. Rembrandt repeats and re-alleges its response to paragraphs 1-30 of the Counterclaims, and further incorporates by reference its allegations in its Complaint filed September 13, 2006.

32. Admitted.

33. Denied.

34. Denied.

35. Denied.

**PRAYER FOR RELIEF**

WHEREFORE, Rembrandt prays that the Court deny in all respects Defendants' prayer for relief, that the Court enter judgment against Defendants on all claims alleged by Defendants, and that the Court enter on behalf of Rembrandt:

- (1) An order that the Defendants have infringed the patents-in-suit;
- (2) An award of damages for said infringement;
- (4) An award of increased damages pursuant to 35 U.S.C. § 284;
- (5) An award of all costs of this action, including attorneys' fees and interest; and
- (6) Such other and further relief, at law or in equity, to which Rembrandt is justly entitled.

Dated: December 15, 2006.

**SUSMAN GODFREY L.L.P.**

By: /s/ Vineet Bhatia

Vineet Bhatia (VB 9964)

SUSMAN GODFREY L.L.P.

590 Madison Ave., 8<sup>th</sup> Floor

New York, NY 10022

Main Telephone: (212) 336-8330

*Attorneys for Plaintiff / Counter-defendant  
Rembrandt Technologies, LP*

**CERTIFICATE OF SERVICE**

I, Tibor Nagy, do hereby certify that on December 15, 2006, a true and correct copy of the Plaintiff's Reply to Defendants' Answer and Counterclaims, dated December 15, 2006, was served by electronic mail and first class mail on:

Roger Netzer  
Willkie Farr & Gallagher LLP  
787 Seventh Avenue  
New York, New York 10019-6099

Attorneys for Defendants/Counterclaimants  
Adelphia Communications Corp. et al.

/s/ Tibor Nagy  
Tibor Nagy

Dated: December 15, 2006

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New York, NY 10022  
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*Attorneys for Plaintiff / Counter-defendant  
Rembrandt Technologies, LP*

**Exhibit E**

**UNITED STATES BANKRUPTCY COURT  
SOUTHERN DISTRICT OF NEW YORK**

<hr/>		<b>X</b>	
		:	
		:	
<b>In re:</b>		:	<b>Chapter 11</b>
		:	
		:	<b>Case No. 02 – 41729 (REG)</b>
		:	
<b>ADELPHIA COMMUNICATIONS CORPORATION., et al.,</b>		:	<b>(Jointly Administered)</b>
		:	
		:	
<b>Debtors.</b>		:	
		:	
		:	
<hr/>		<b>X</b>	

**STIPULATED ORDER ESTABLISHING SEPARATE RESERVE FOR  
REMBRANDT TECHNOLOGIES, LP ADMINISTRATIVE CLAIM**

WHEREAS, on September 13, 2006, Rembrandt Technologies, LP (“Rembrandt”) commenced an adversary proceeding against Adelphia Communications Corporation and certain of its subsidiaries and affiliates alleging post-petition patent infringement and filed an administrative claim in the above-captioned case with respect to the damages arising from such alleged infringement (the “Rembrandt Administrative Claim”).<sup>1</sup>

WHEREAS, the Debtors dispute the Rembrandt Administrative Claim and intend to vigorously defend against it; and

WHEREAS, this Court has scheduled a hearing for the purpose of estimating the Rembrandt Administrative Claim solely for the purpose of determining the amount of cash to be reserved in respect of such claim upon the occurrence of the Effective Date of the Plan; and

WHEREAS, on November 22, 2006, Rembrandt filed an objection to confirmation of the Plan (the “Rembrandt Plan Objection”), requesting that this Court condition confirmation of the Plan upon the establishment of a cash reserve that would be used solely to

<sup>1</sup> Capitalized terms not defined herein shall have the meanings attributed to them in the Fifth Amended Joint Chapter 11 Plan for Adelphia Communications Corporation and Certain Affiliated Debtors, dated October 16, 2006 (as may be further modified or amended, the “Plan”).

satisfy the Rembrandt Administrative Claim upon such claim becoming an Allowed Administrative Claim; and

WHEREAS, the Debtors and Rembrandt have engaged in negotiations and agreed on the amount of cash to be reserved in respect of the Rembrandt Administrative Claim.

NOW, THEREFORE, IT IS HEREBY:

**ORDERED**, that on the Effective Date of the Plan, the Debtors shall establish a separate reserve that shall be maintained and used as set forth herein (the "Dedicated Rembrandt Reserve"), and such reserve shall be funded in the amount of \$35 million; and it is hereby

**ORDERED**, that pursuant to the Plan and as shall be provided in the Confirmation Order, the Plan Administrator shall disburse funds from the Dedicated Rembrandt Reserve to Rembrandt to the extent that the Rembrandt Administrative Claim becomes an Allowed Administrative Claim, and the Plan Administrator shall only use such funds for any other purpose pursuant to the Plan (a) after the Rembrandt Administrative Claim is fully adjudicated pursuant to a Final Order and (b) after the Allowed Rembrandt Administrative Claim is paid in full; and it is hereby

**ORDERED**, that this Stipulated Order and the establishment of the Dedicated Rembrandt Reserve are without prejudice to Rembrandt's right to obtain payment from all other available sources of cash under, and pursuant to, the Plan, to the extent that there are any such sources beginning as of the date that the Rembrandt Administrative Claim becomes Allowed, in the event that the Rembrandt Administrative Claim is Allowed in an amount greater than the funds held in the Dedicated Rembrandt Reserve; and it is hereby

**ORDERED**, that no provision of this Stipulated Order shall be deemed an admission of liability with respect to the Rembrandt Administrative Claim or an admission as to the ultimate amount of damages properly attributable to that Claim, and this Stipulated Order shall be without prejudice to the respective litigation positions of the parties hereto, and it is hereby

**ORDERED**, that subject to the terms of this Stipulated Order, the Rembrandt Plan Objection shall be deemed withdrawn with prejudice.

Dated: December 13, 2006

*S/ Robert E. Gerber*  
HONORABLE ROBERT E. GERBER  
UNITED STATES BANKRUPTCY JUDGE

Dated: December 12, 2006

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